

Fig. 1

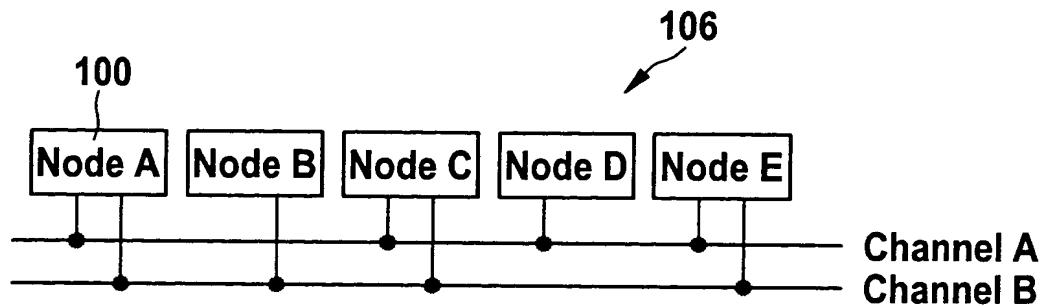


Fig. 2

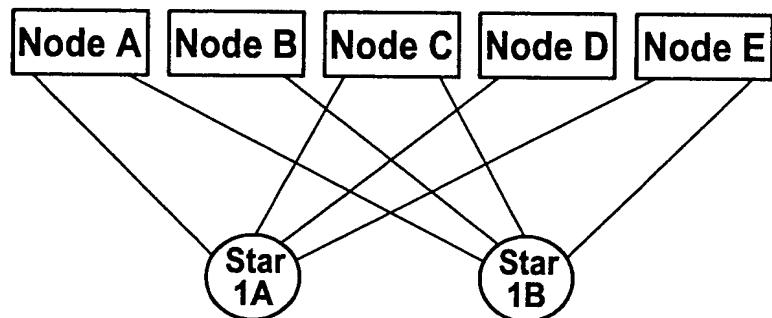


Fig. 3

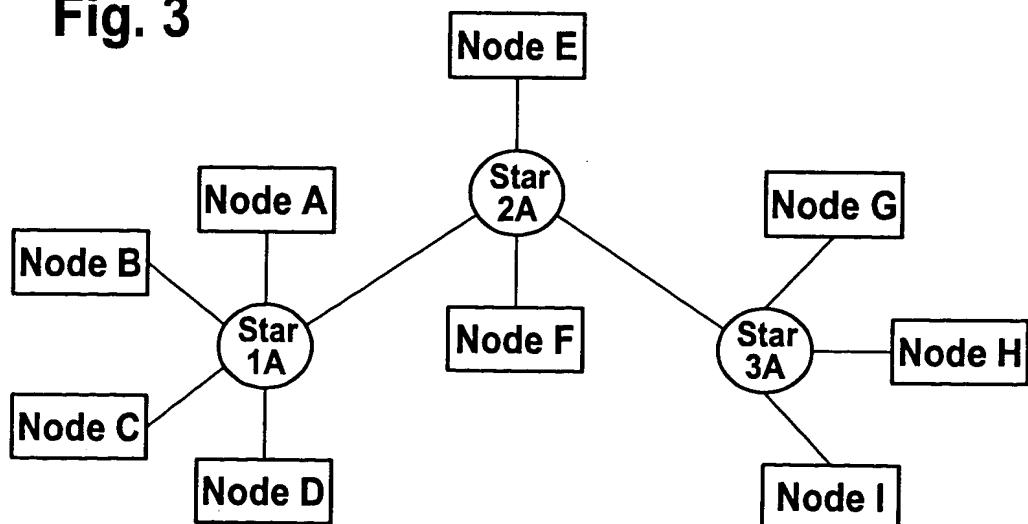


Fig. 4

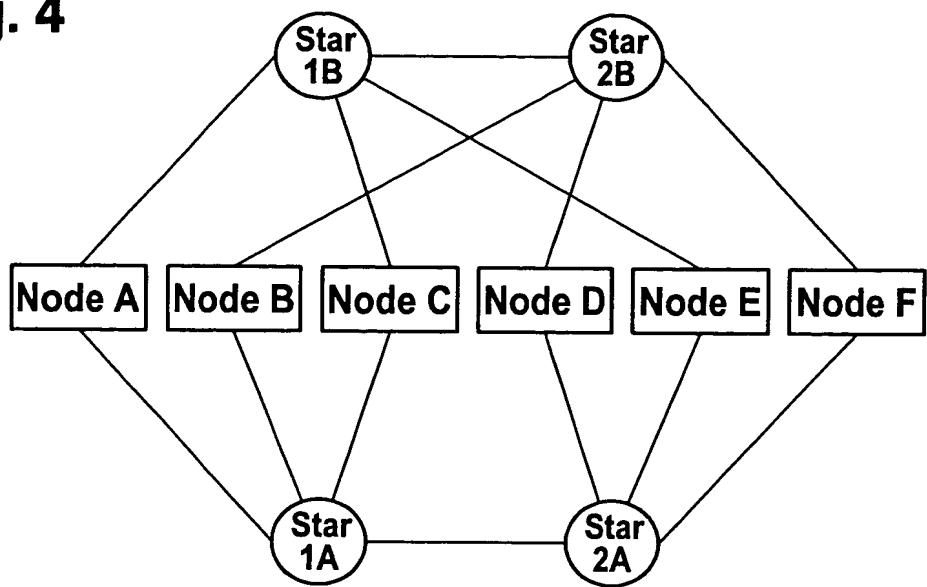


Fig. 5

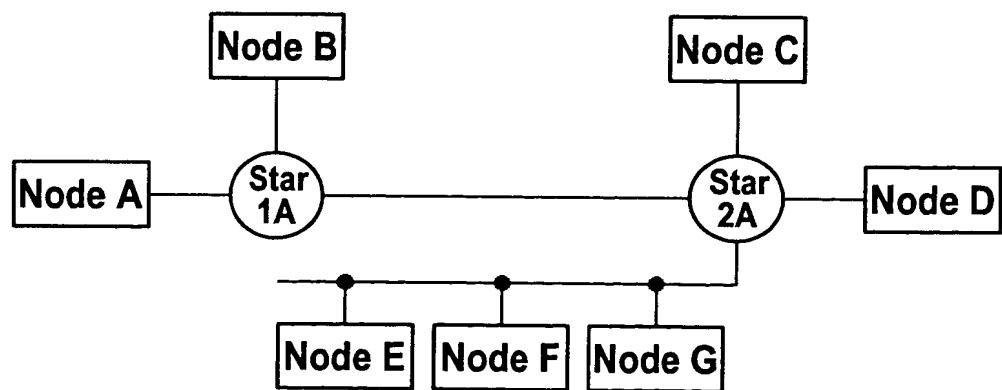


Fig. 6

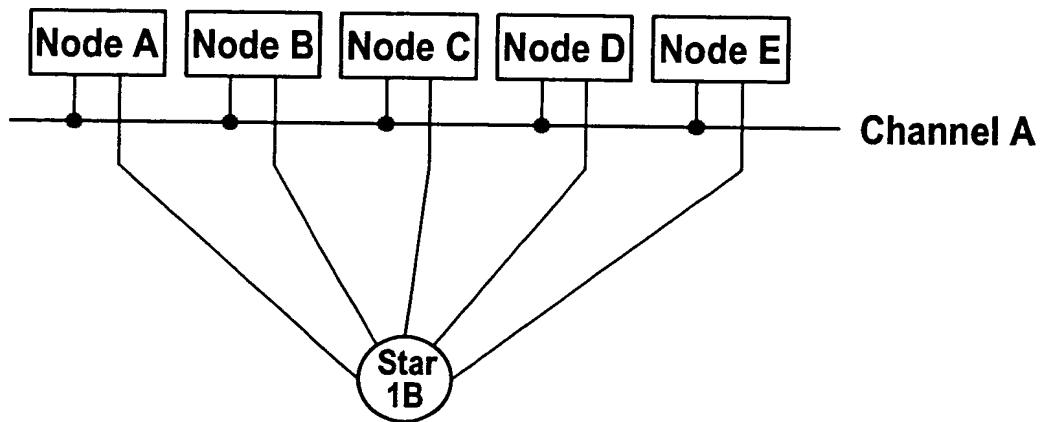


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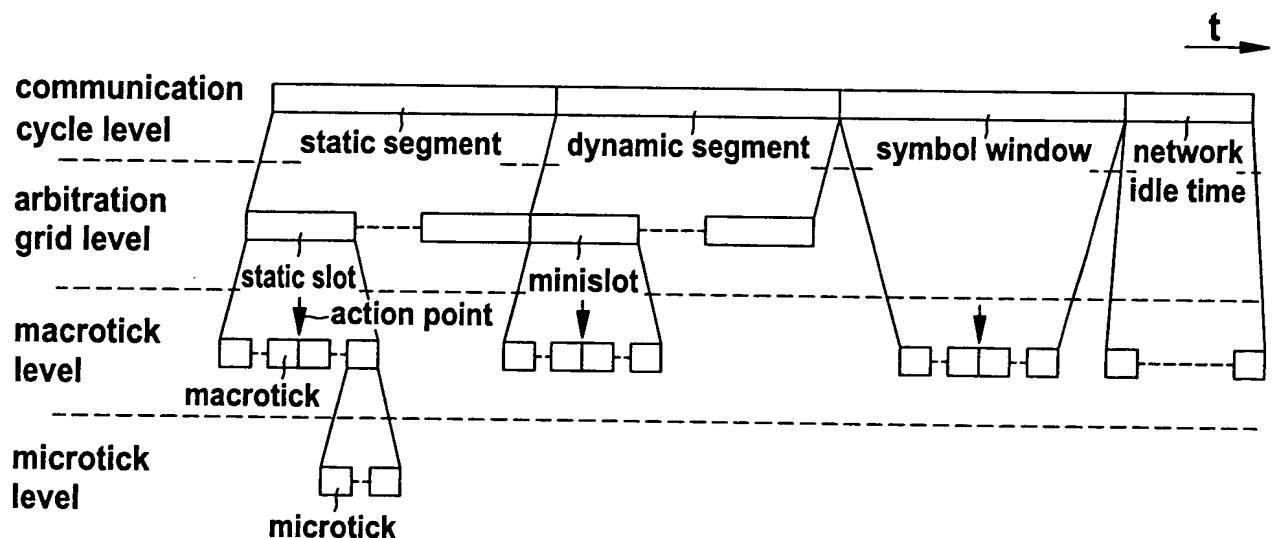


Fig. 8

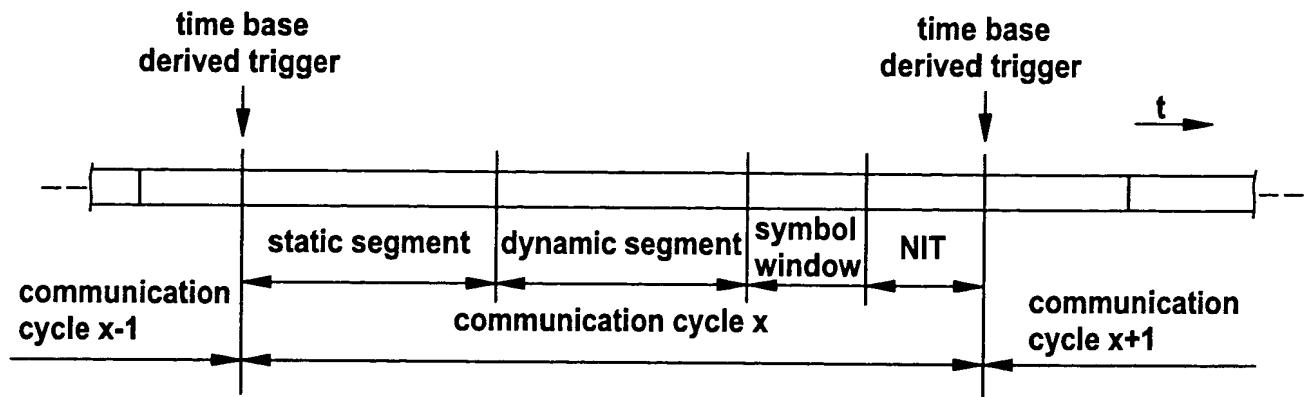


Fig. 9

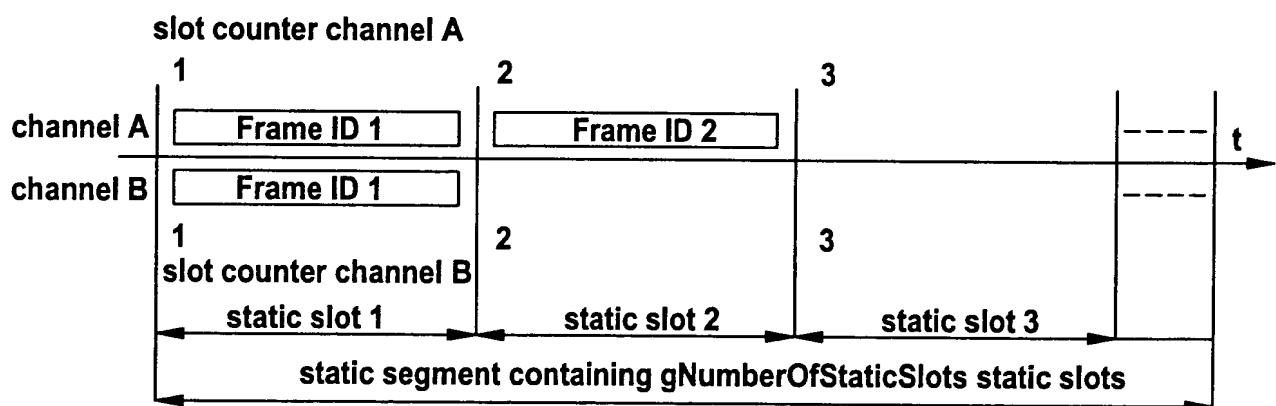


Fig. 10

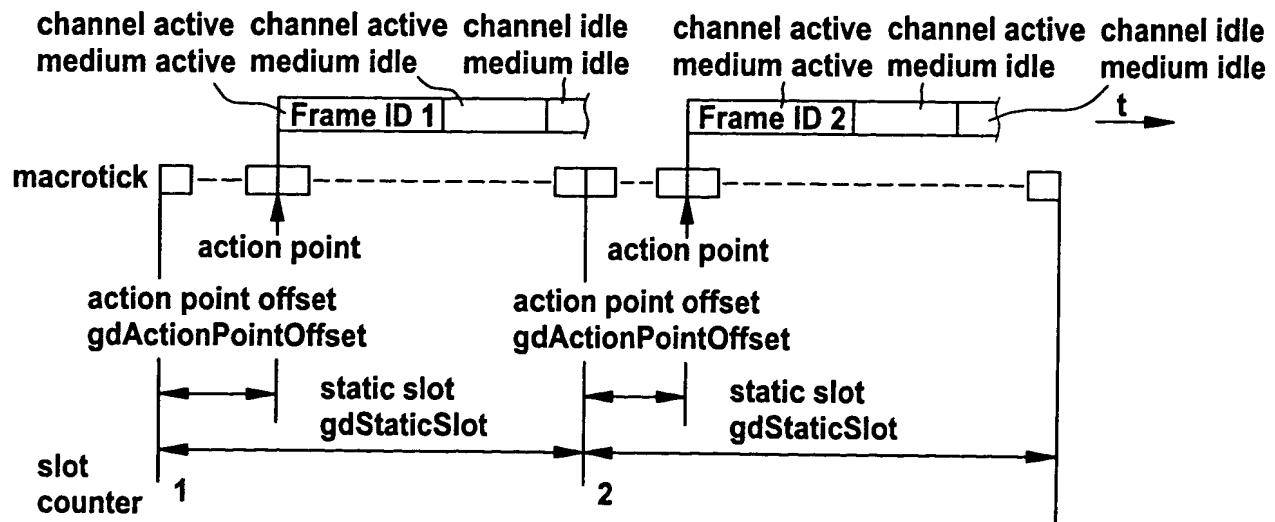


Fig. 11

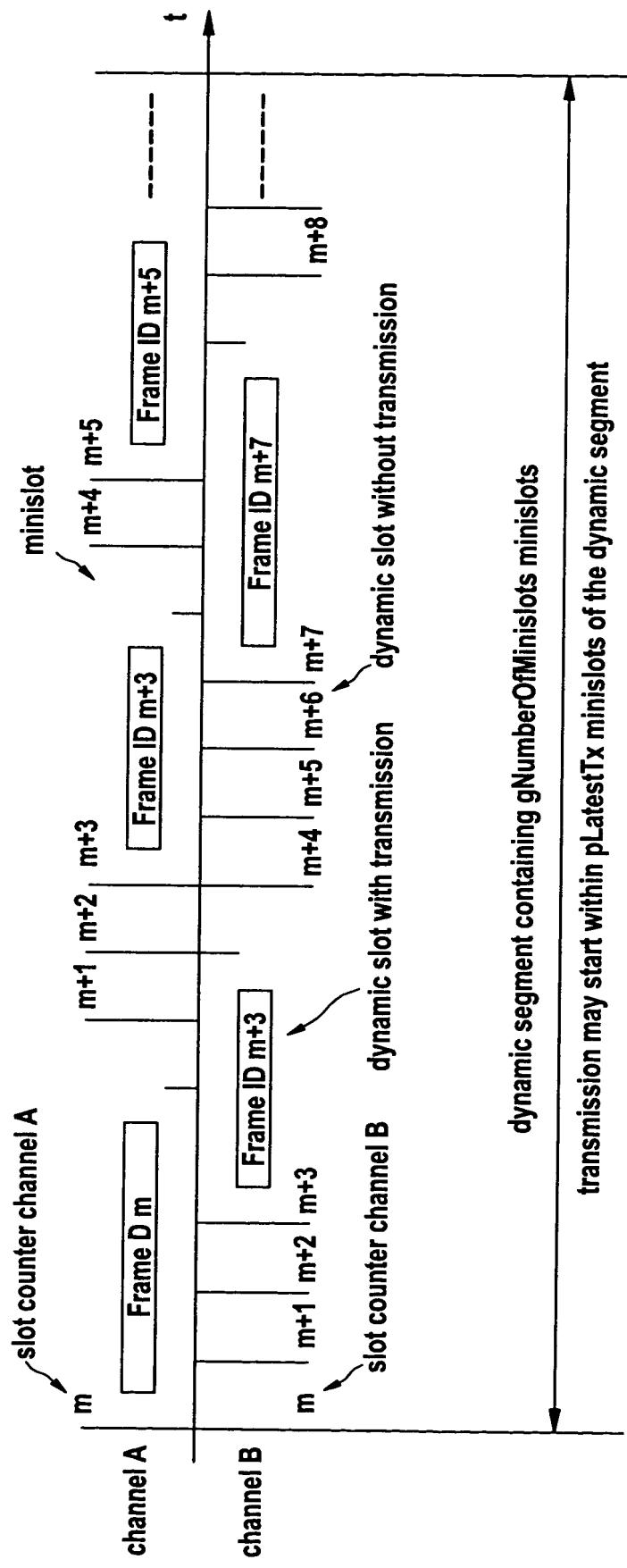


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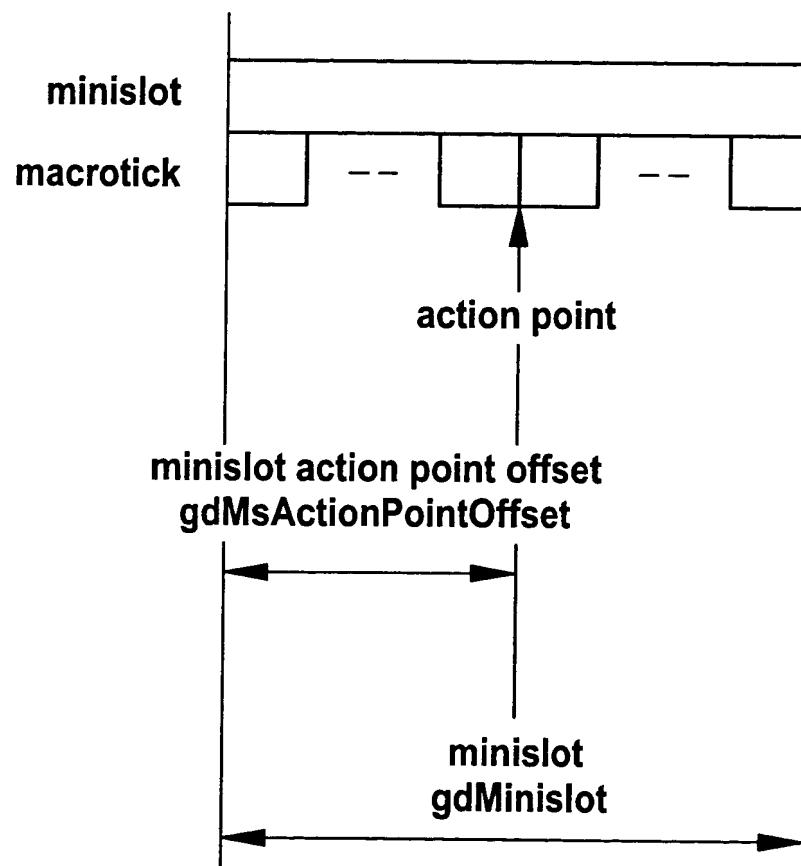


Fig. 13

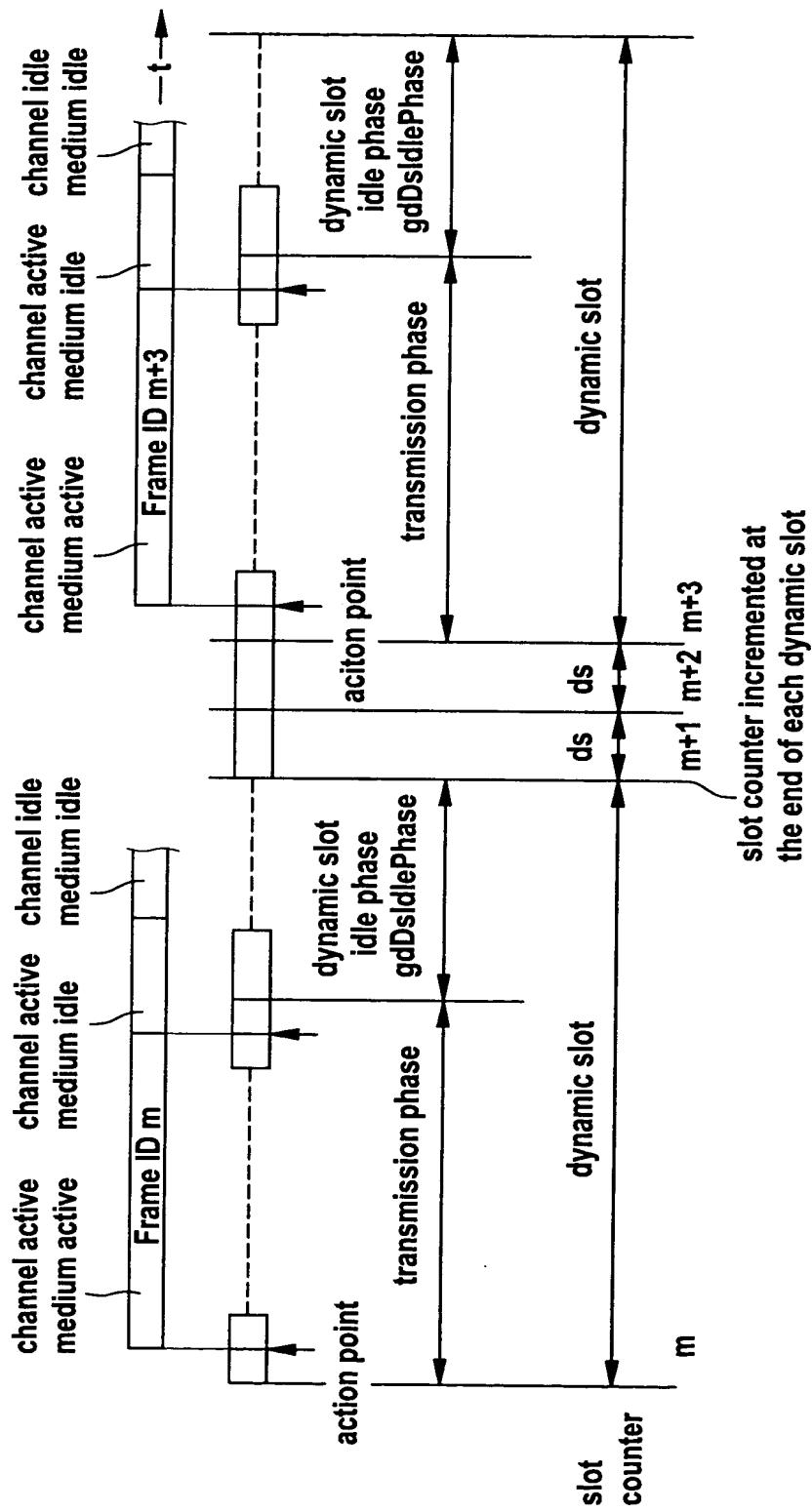


Fig. 14

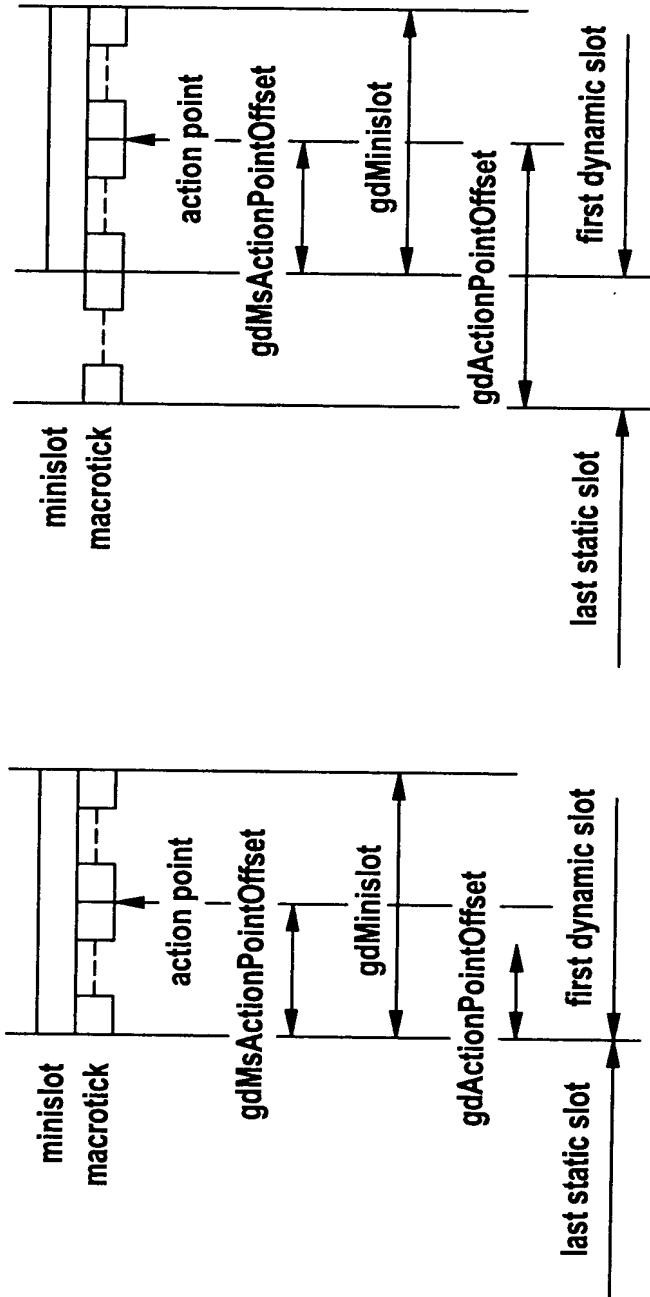


Fig. 15

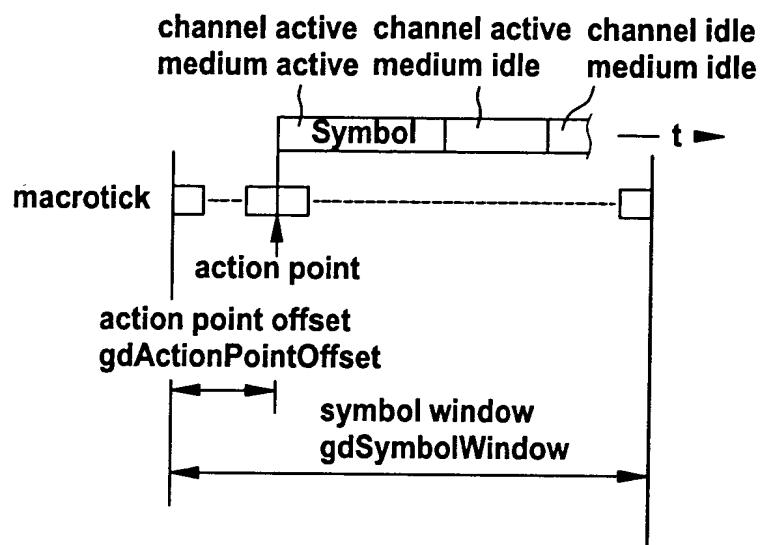


Fig. 16

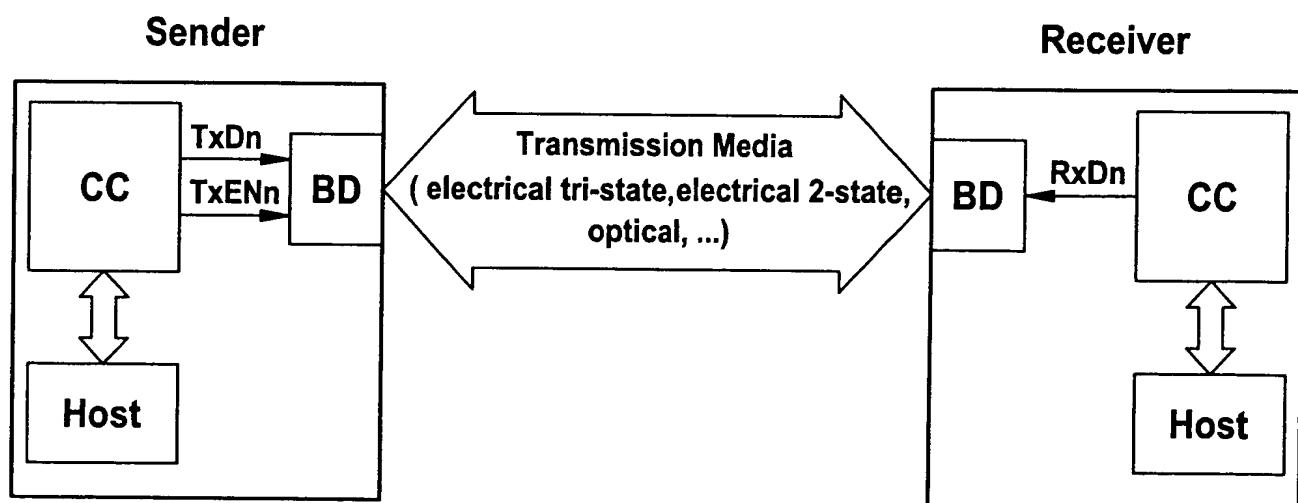


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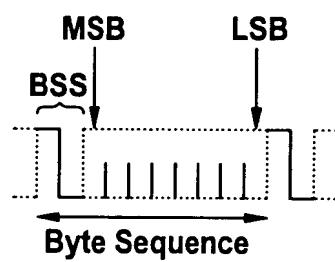


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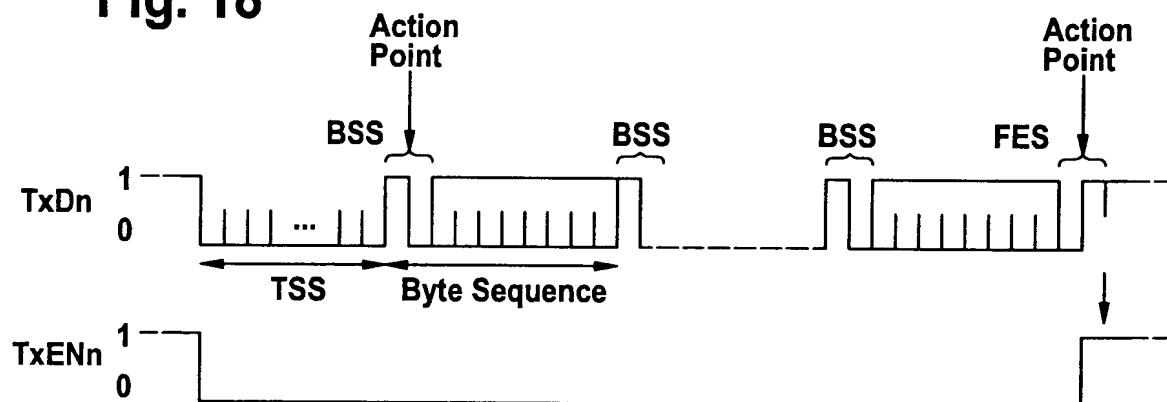


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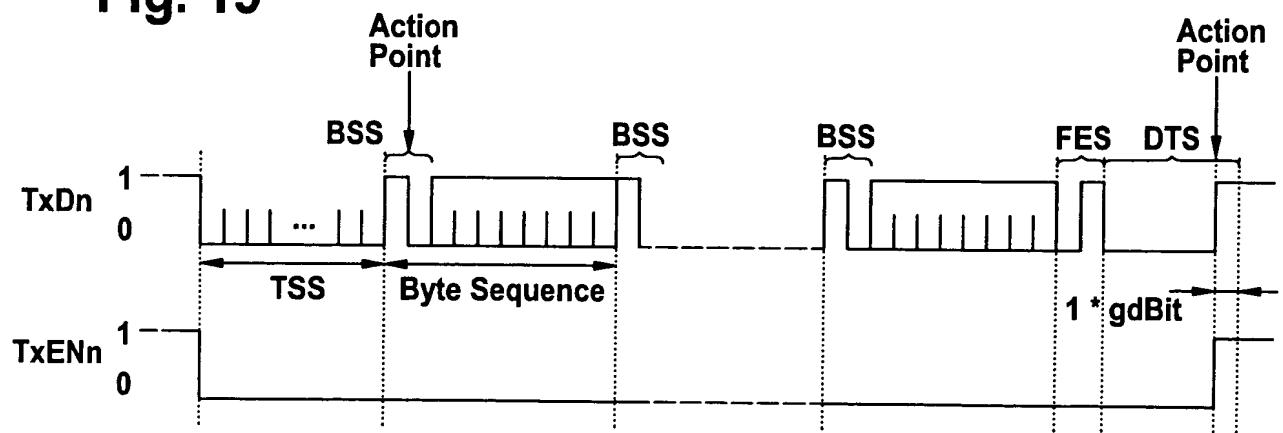


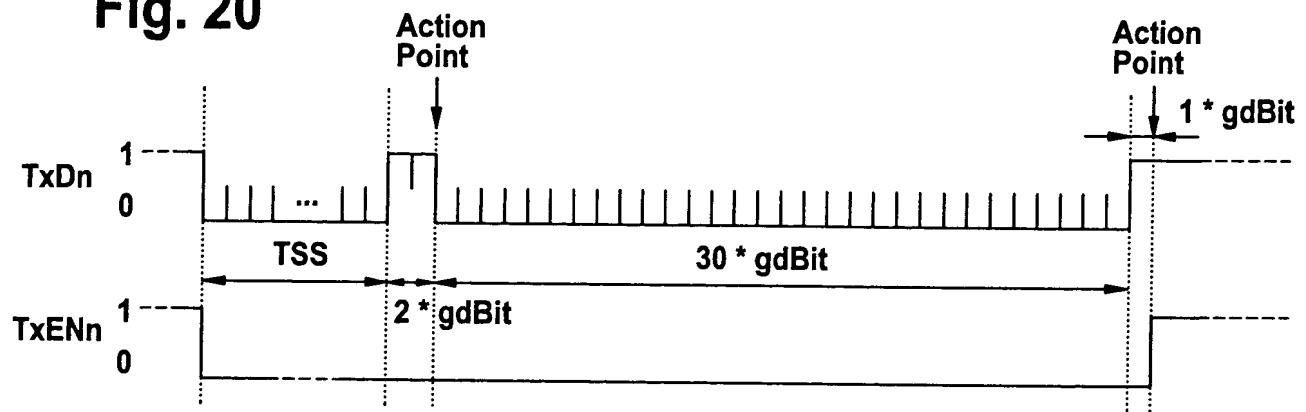
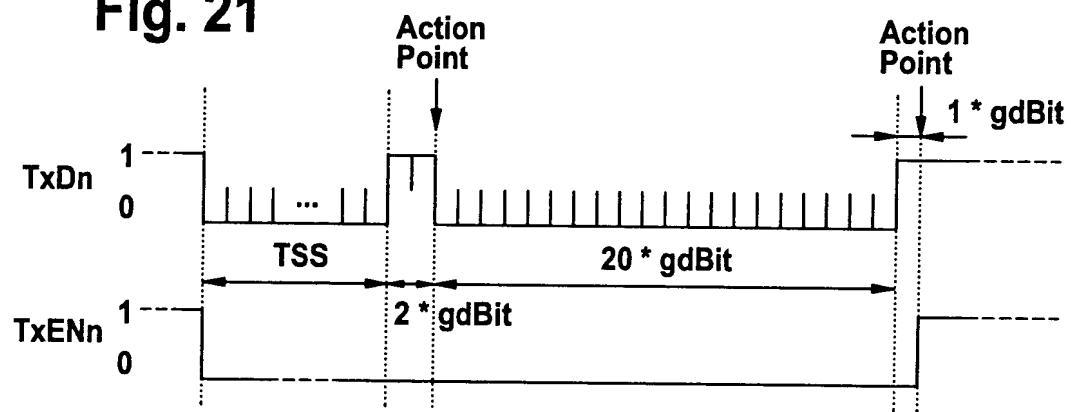
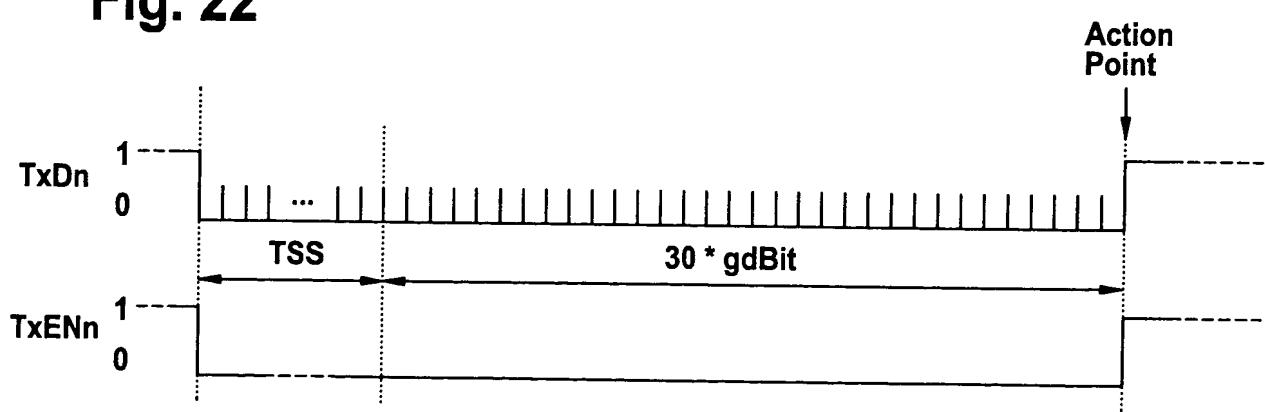
Fig. 20**Fig. 21****Fig. 22**

Fig. 23

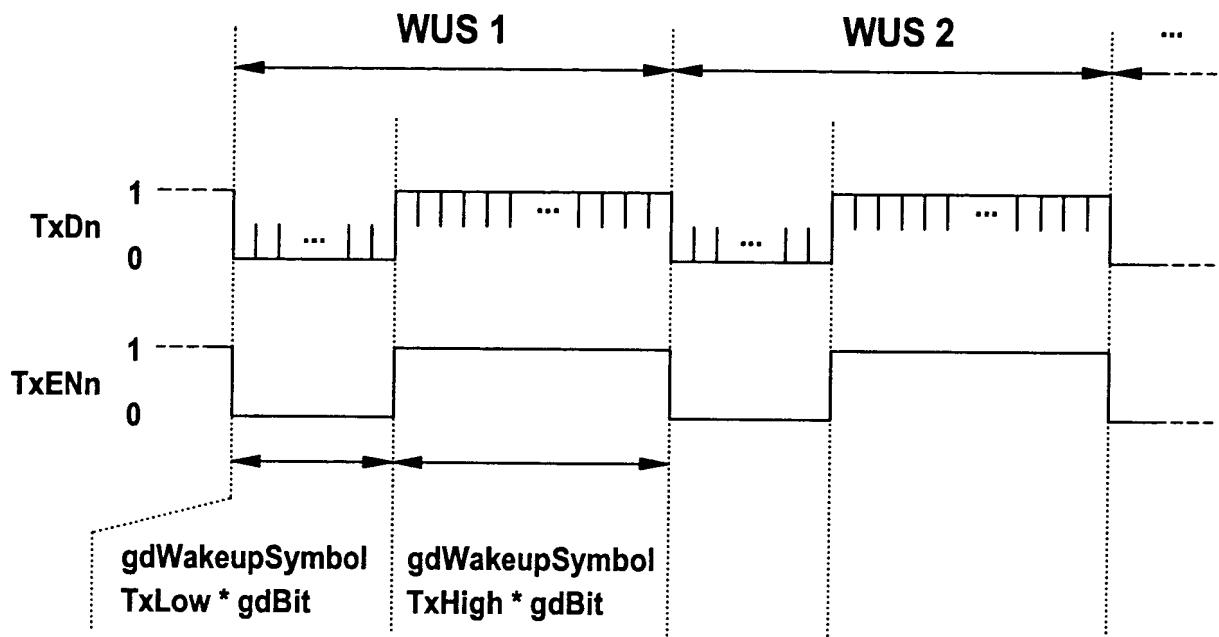


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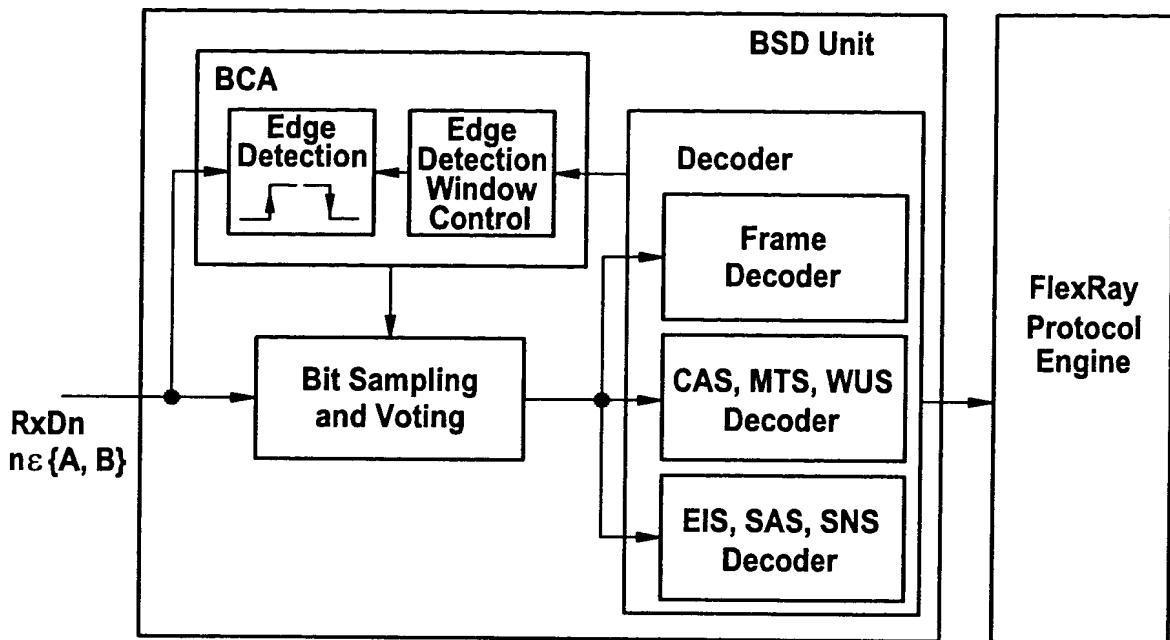


Fig. 25

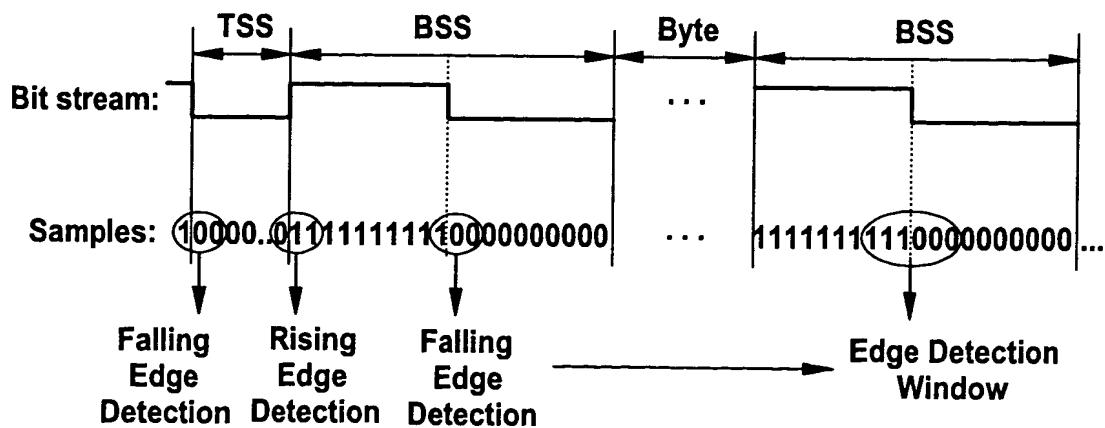


Fig. 26

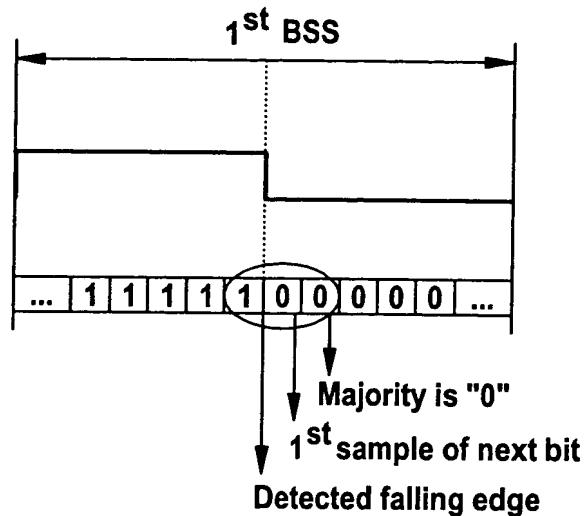


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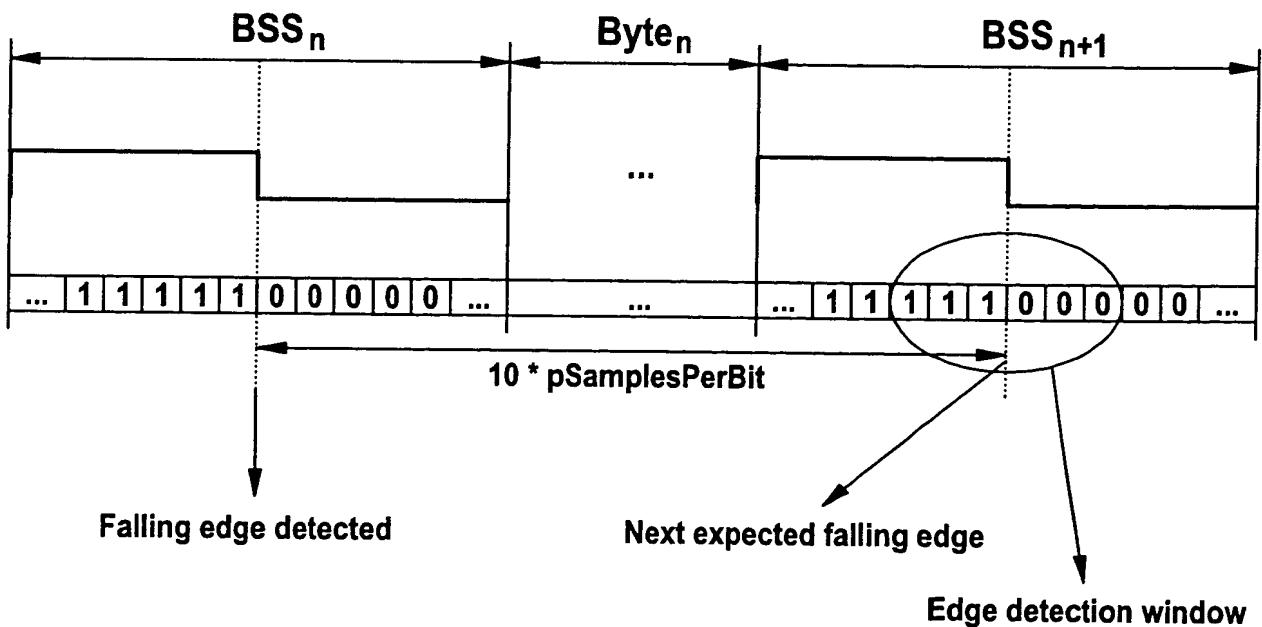


Fig. 28

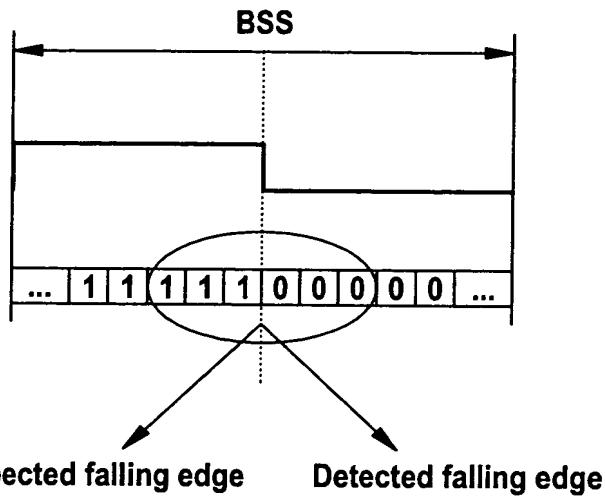


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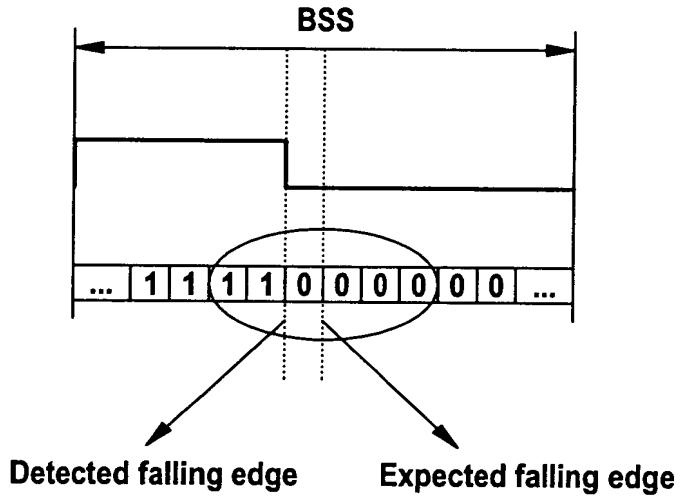


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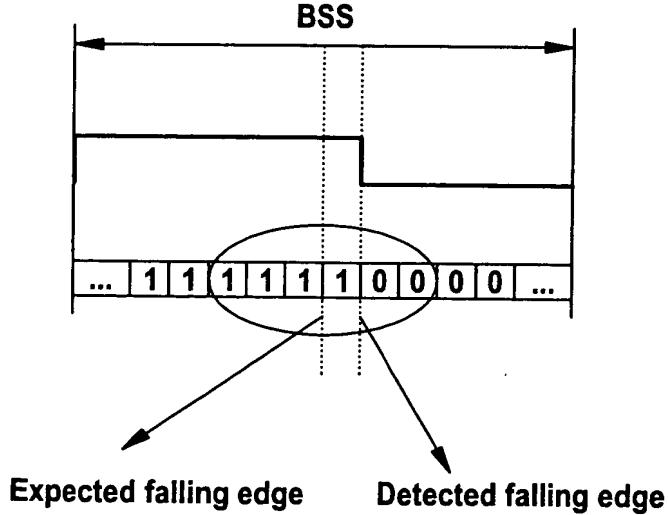


Fig. 31

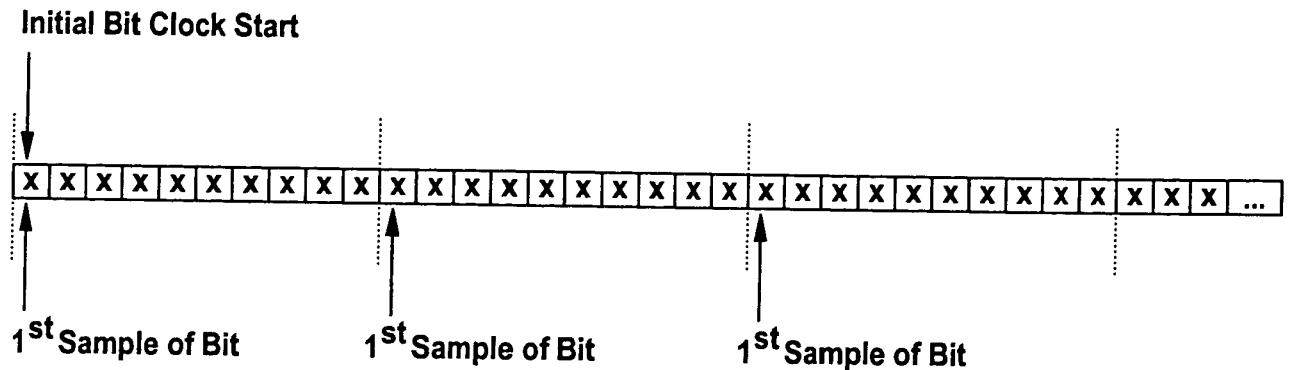


Fig. 32

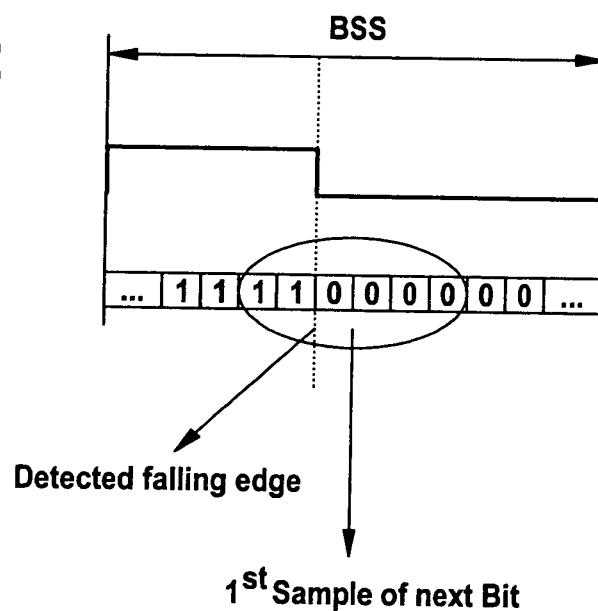


Fig. 33

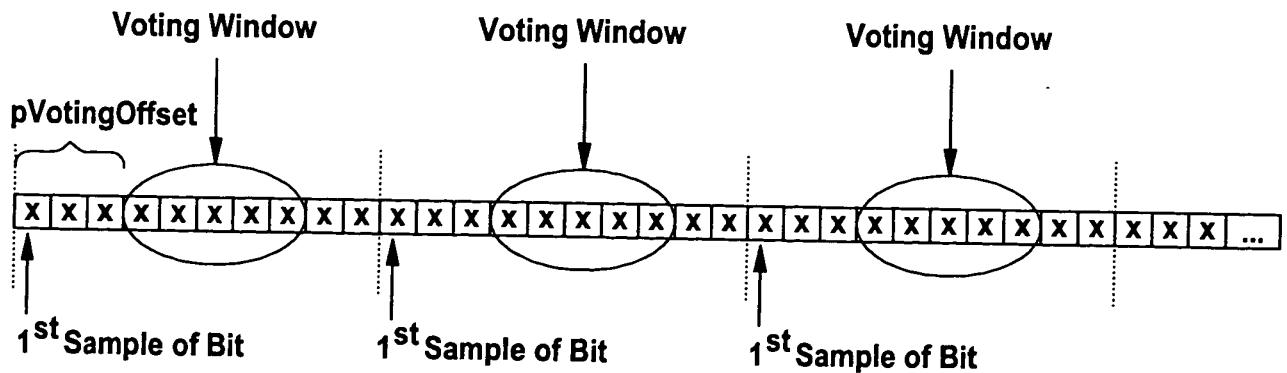


Fig. 34

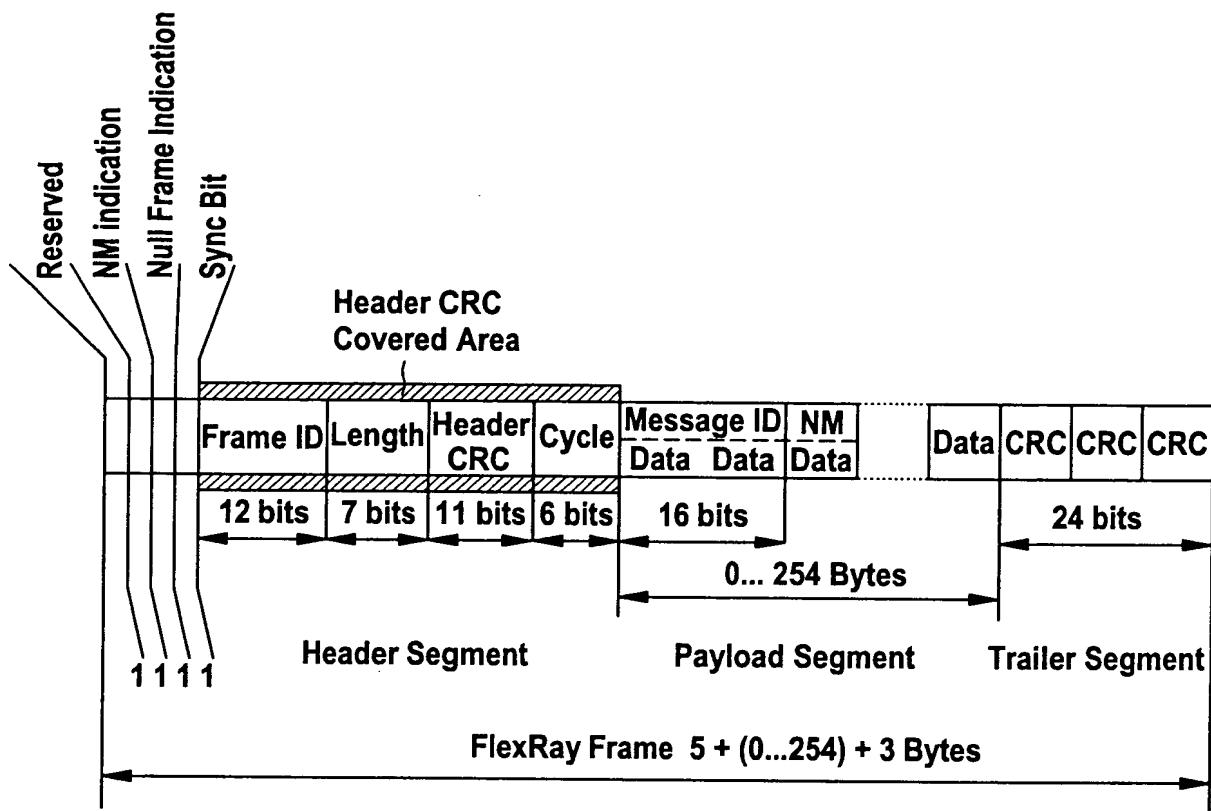


Fig. 35

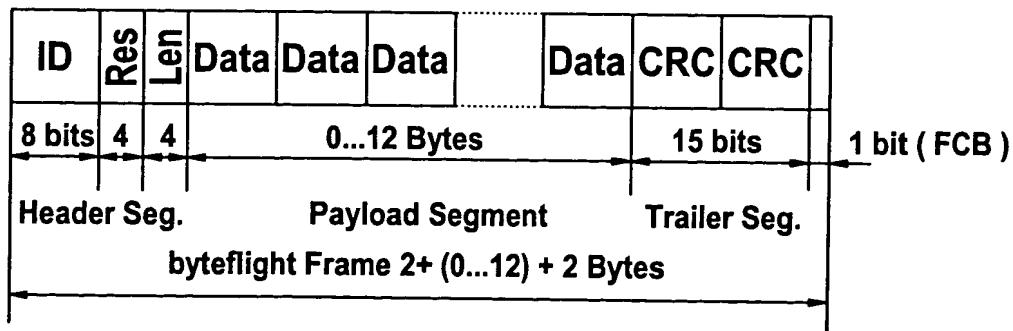


Fig. 36

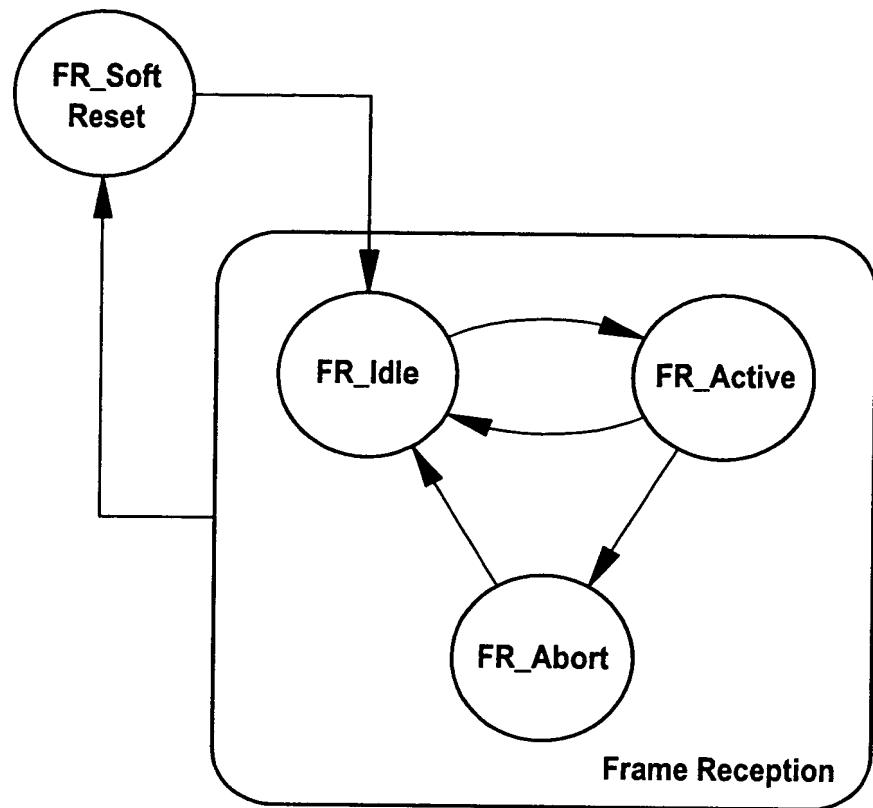


Fig. 37

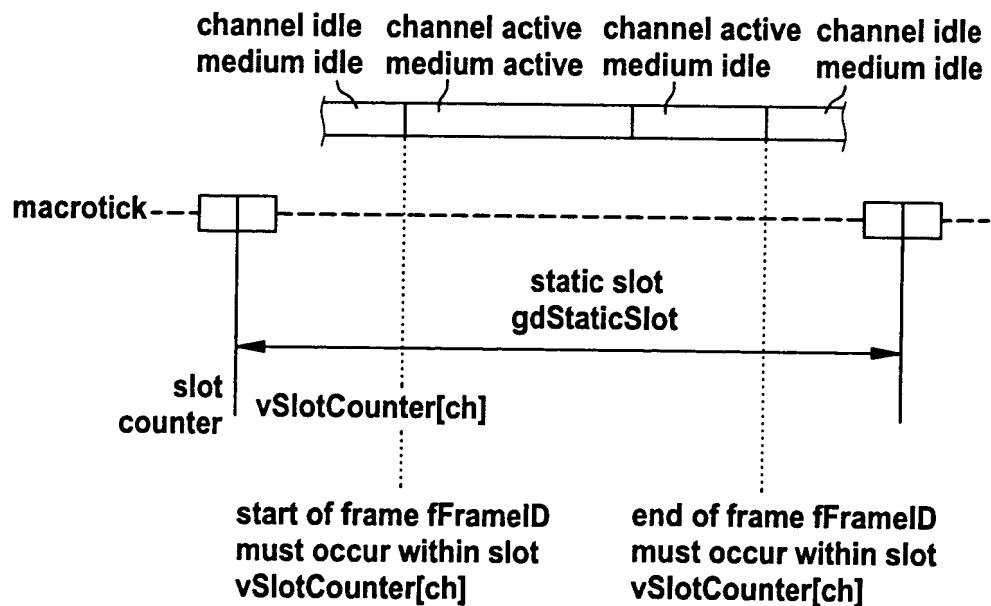


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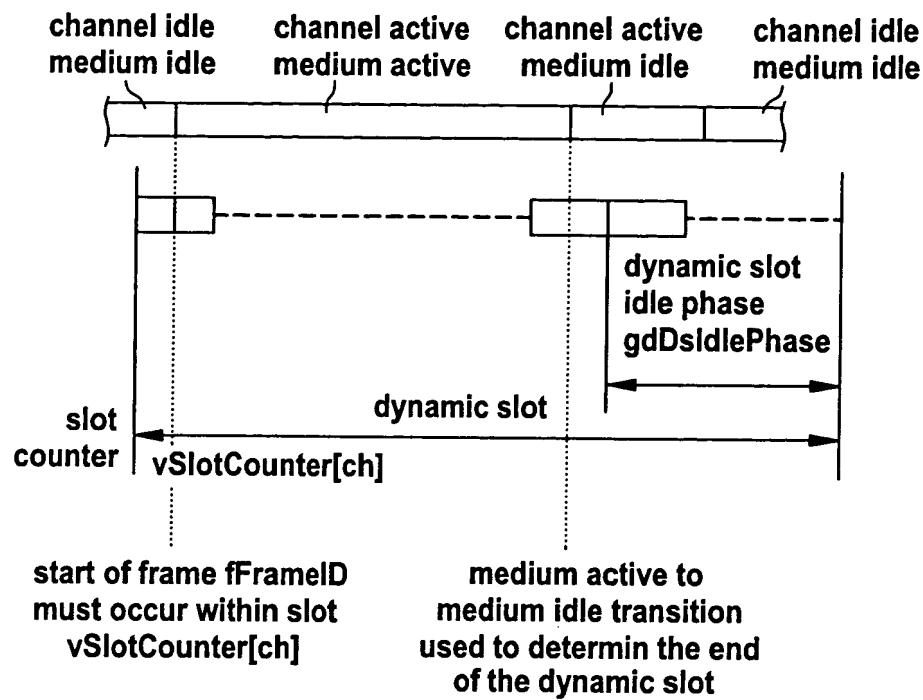
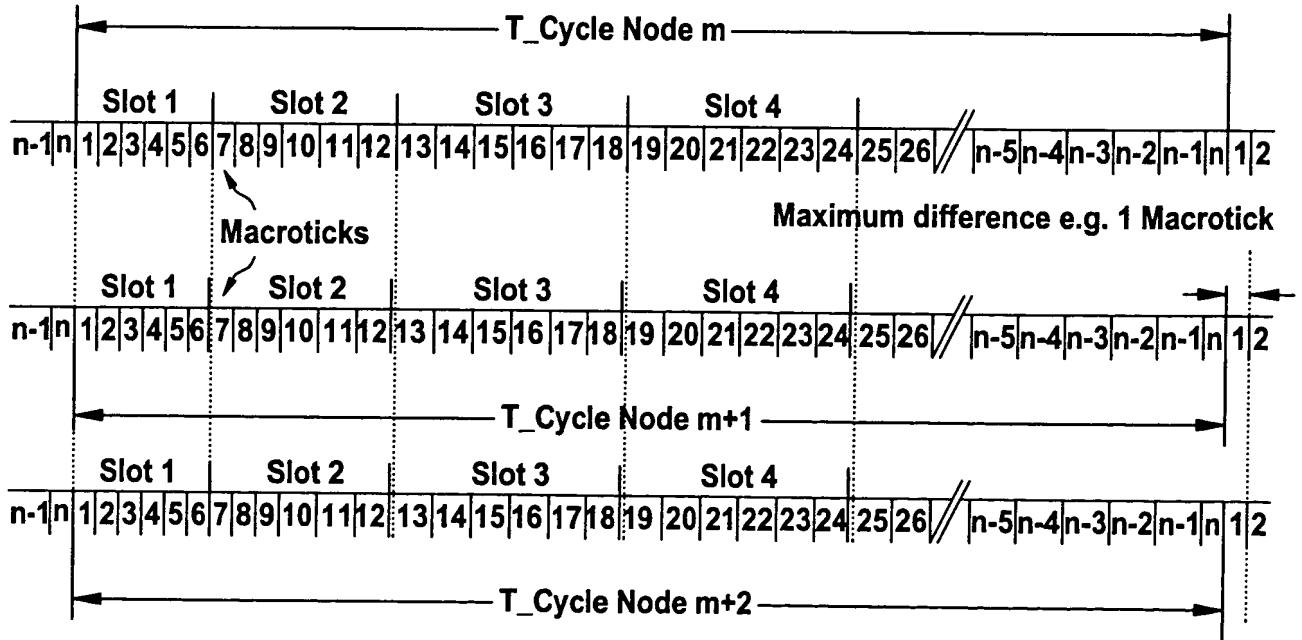


Fig. 39



n = number of Macroticks per cycle

Fig. 40

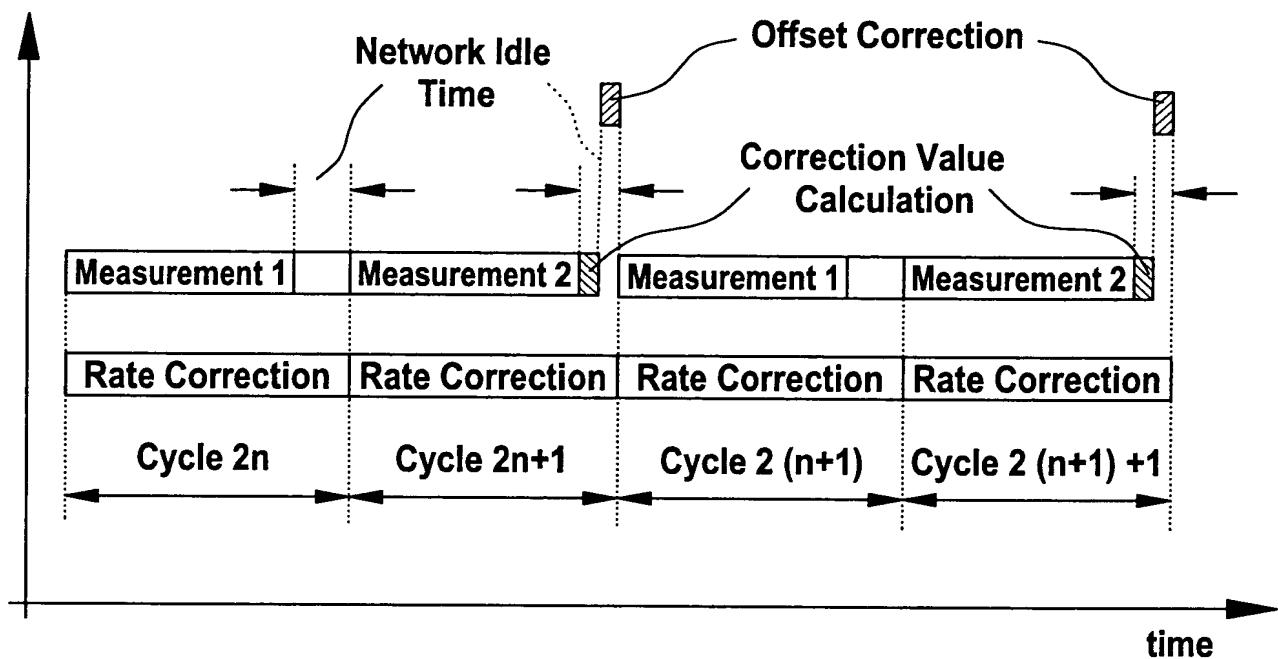


Fig. 41

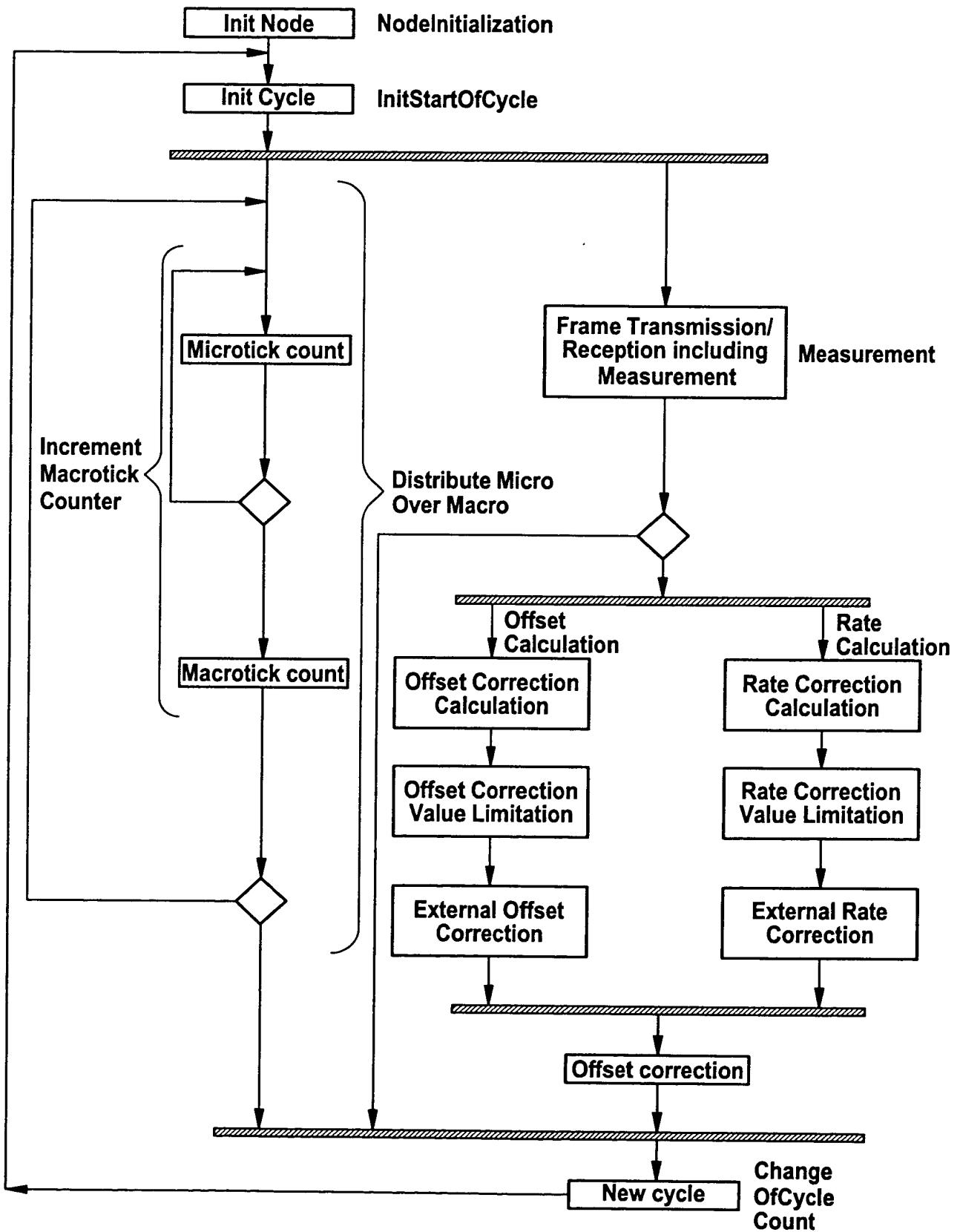


Fig. 42

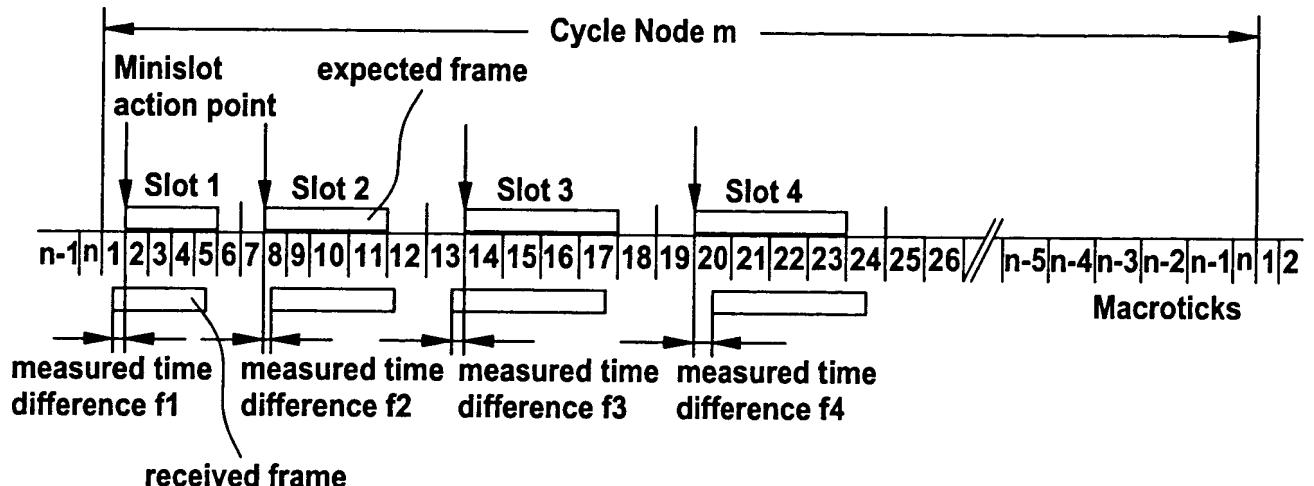


Fig. 43

$$\begin{array}{r}
 15 \\
 13 \\
 11 \\
 \dots \\
 6 \\
 3 \\
 -5
 \end{array}
 \rightarrow + \rightarrow 17 / 2 = 8$$

Fig. 44

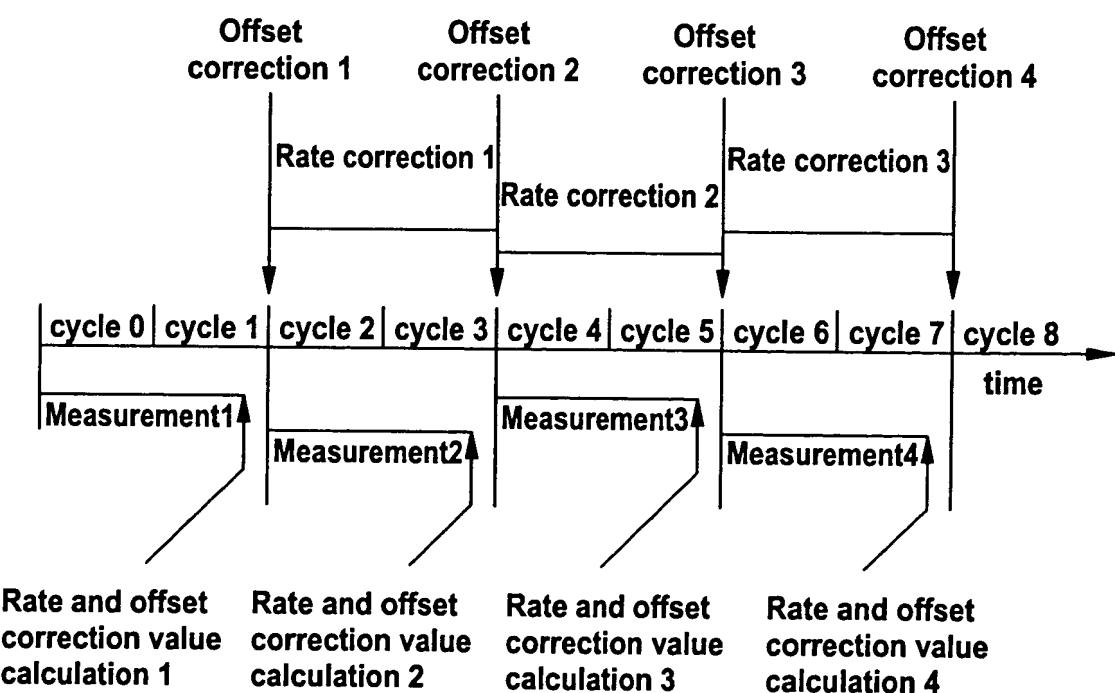


Fig. 45

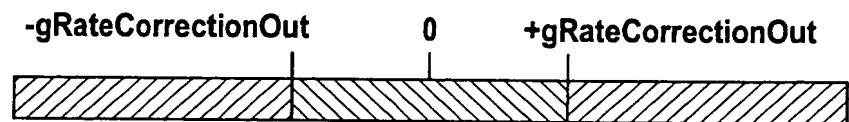


Fig. 46

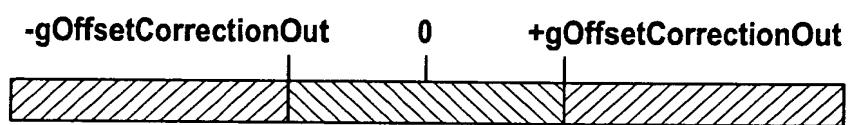


Fig. 47

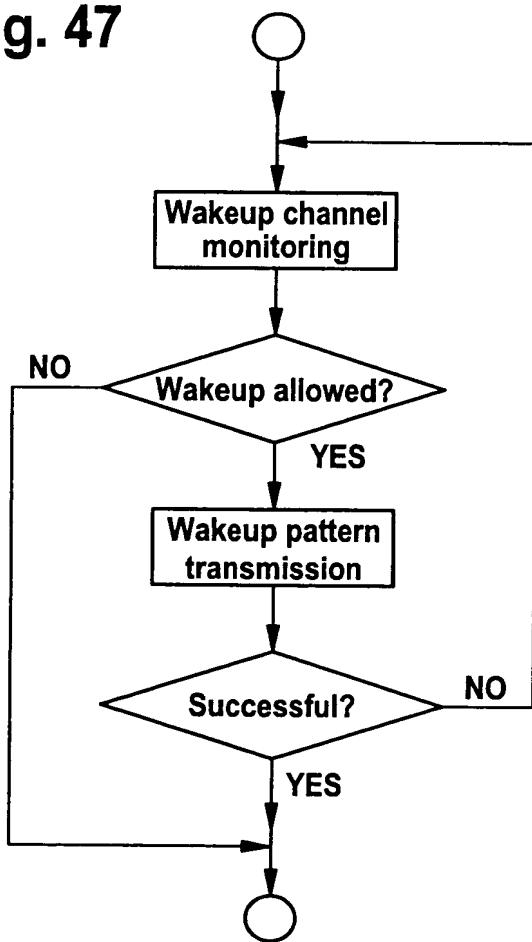


Fig. 48

Wakeup channel monitoring

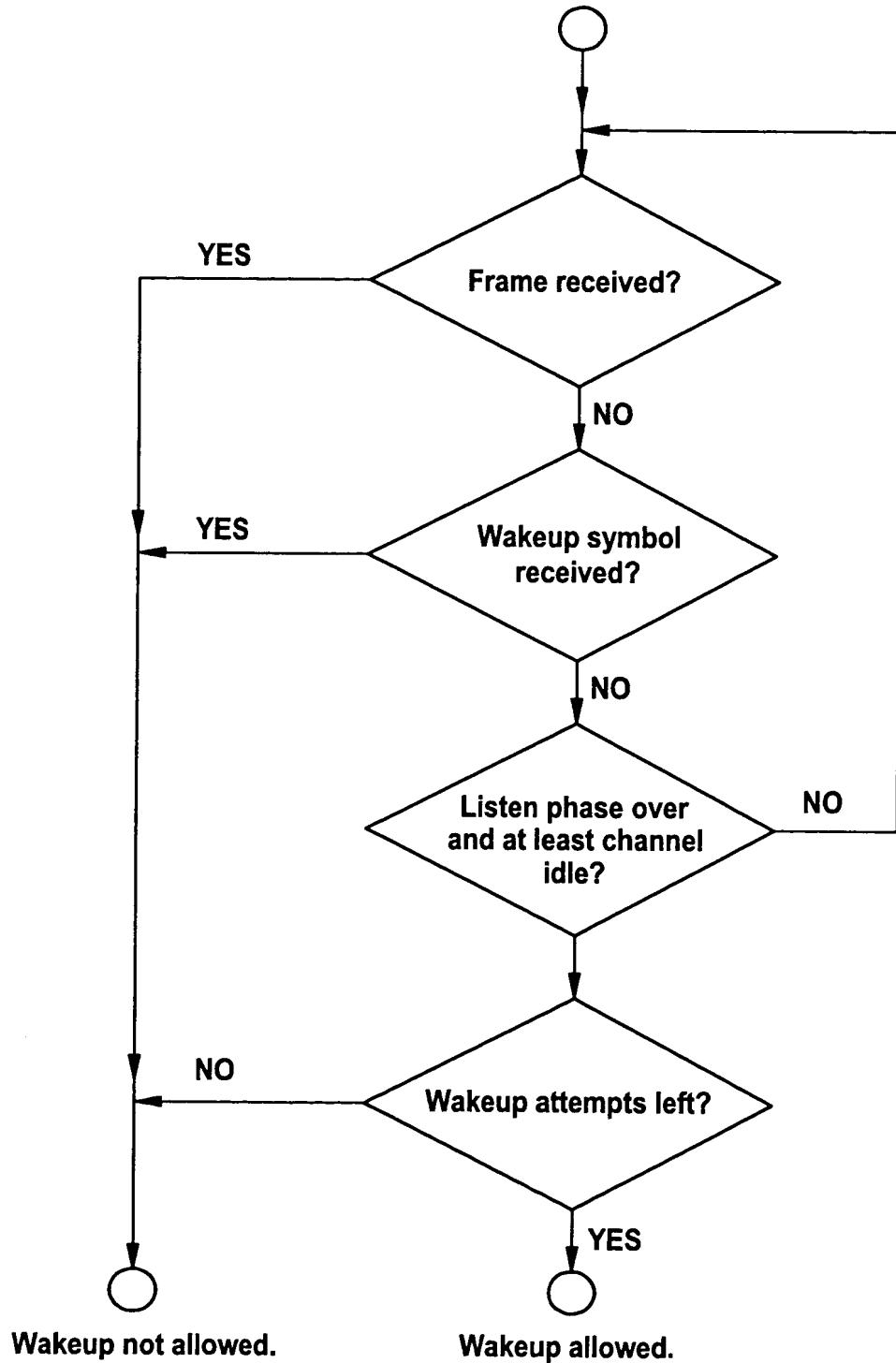


Fig. 49
Wakeup pattern transmission

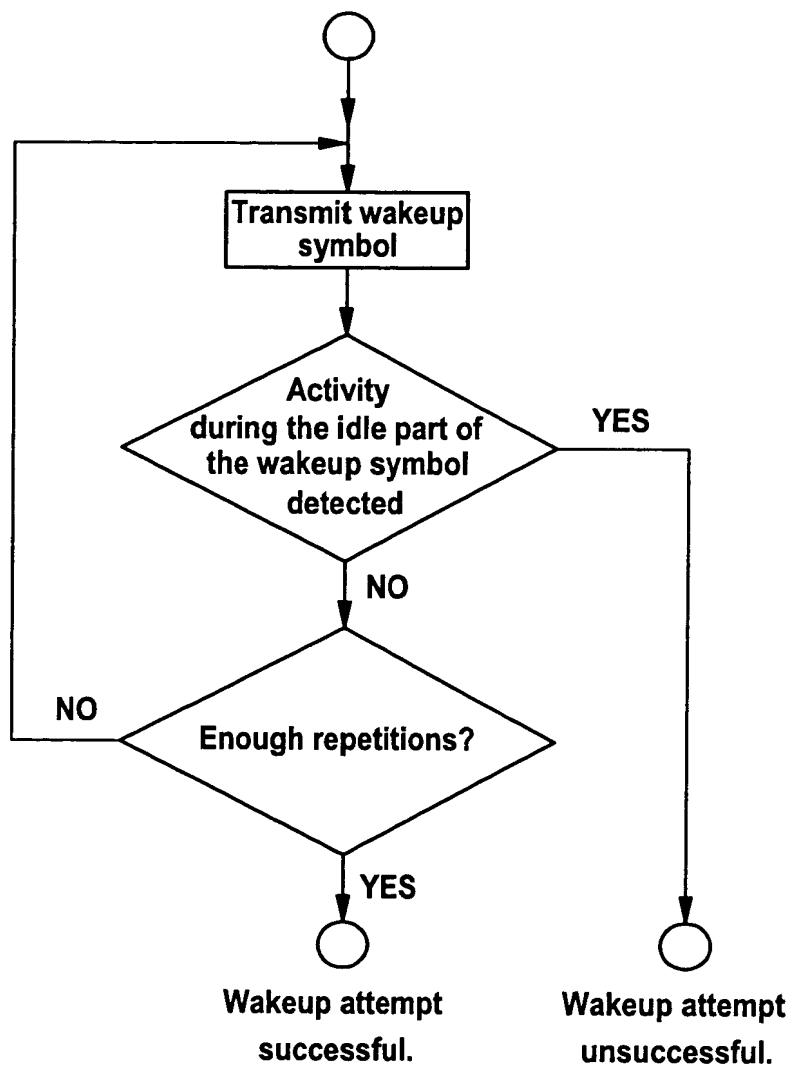


Fig. 50

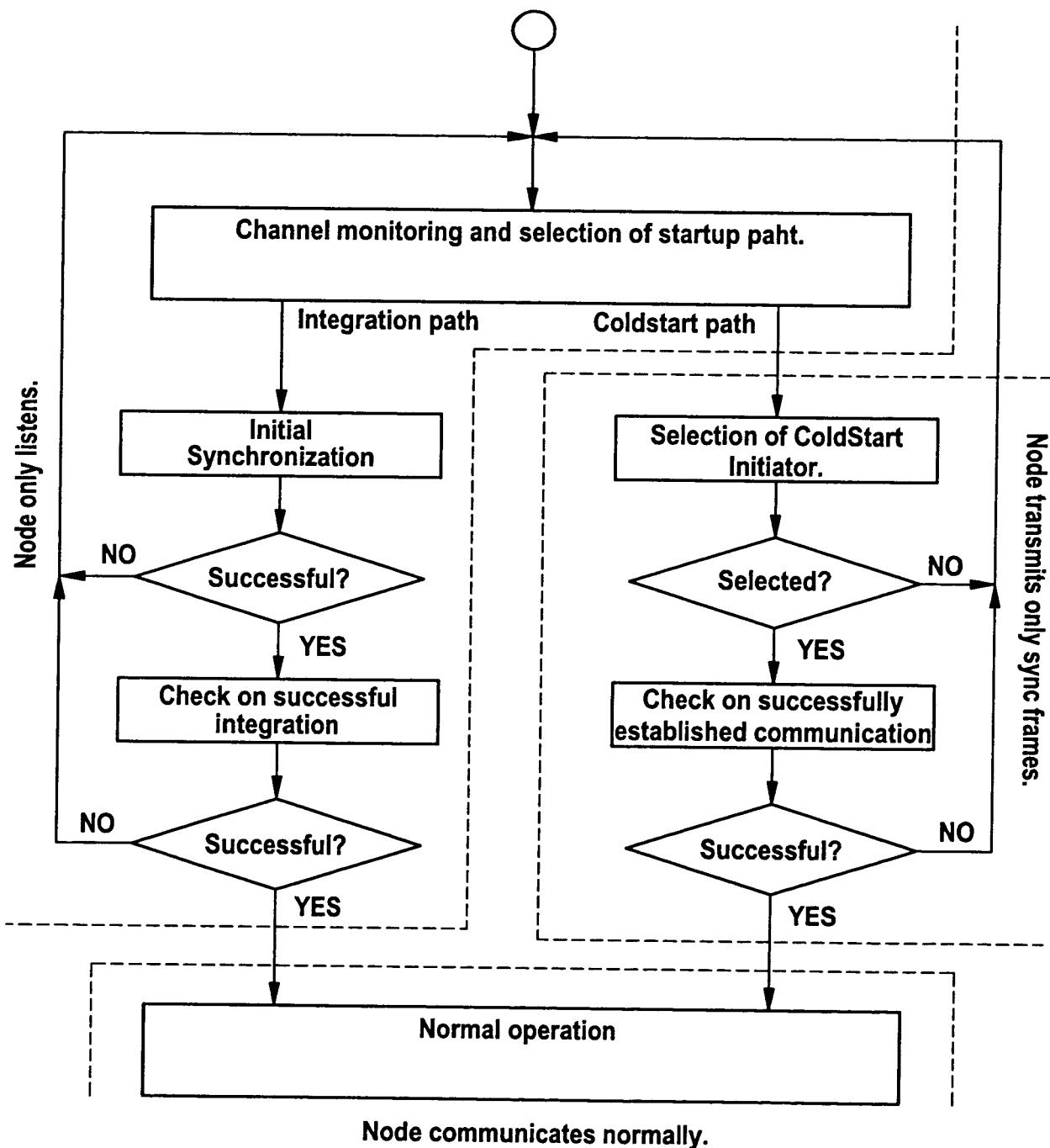


Fig. 51

Channel monitoring and selection of startup path.

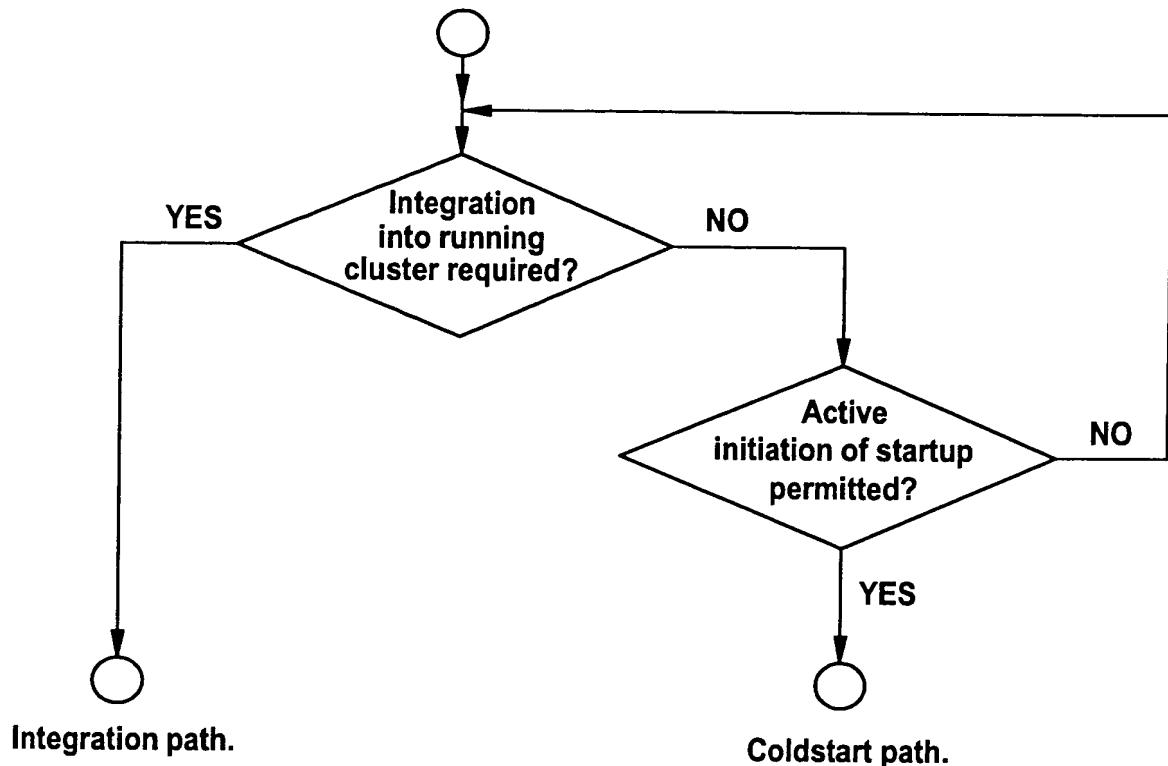


Fig. 52
Selection of ColdStart Initiator

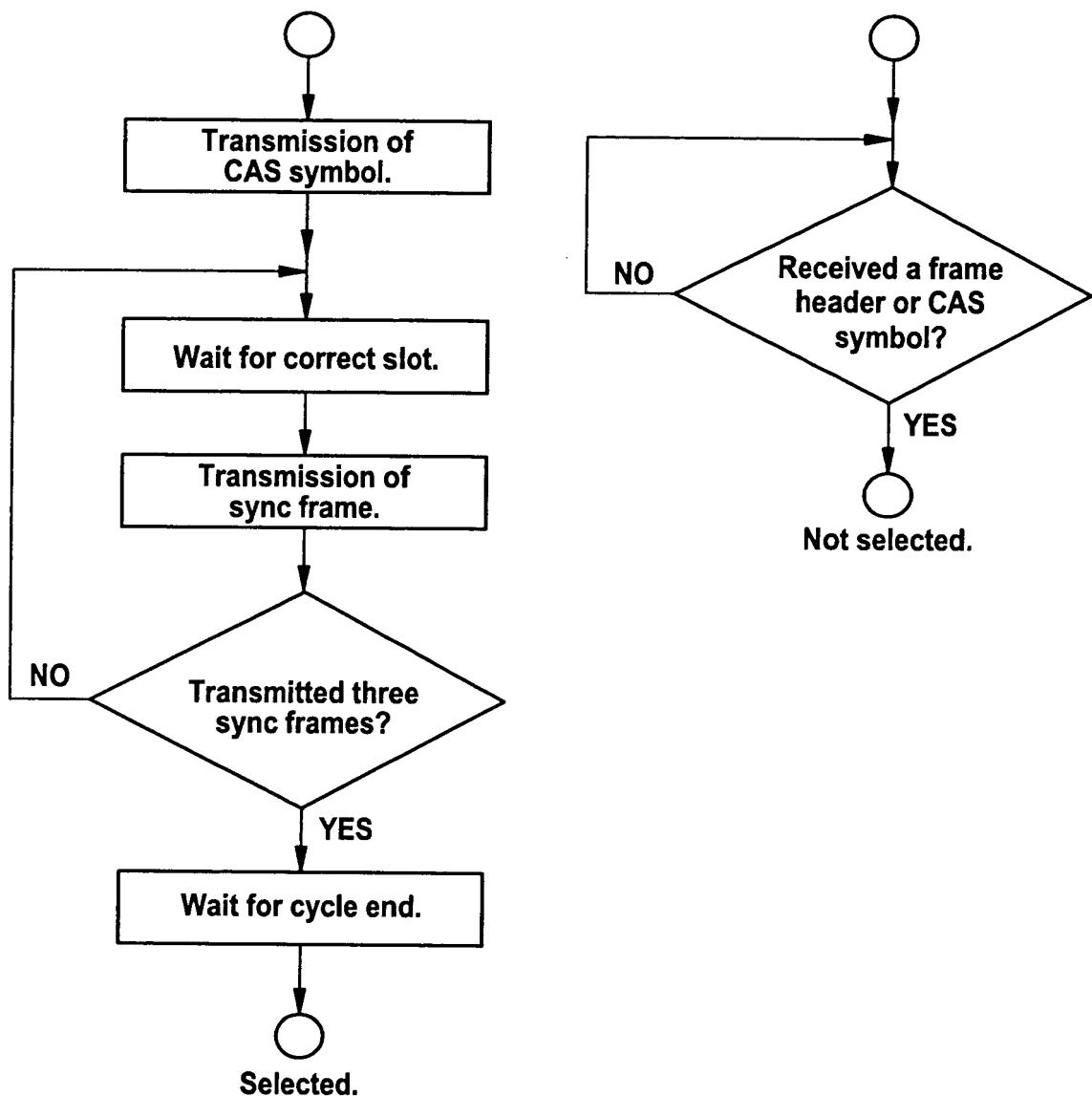


Fig. 53

Check on successfully established communication

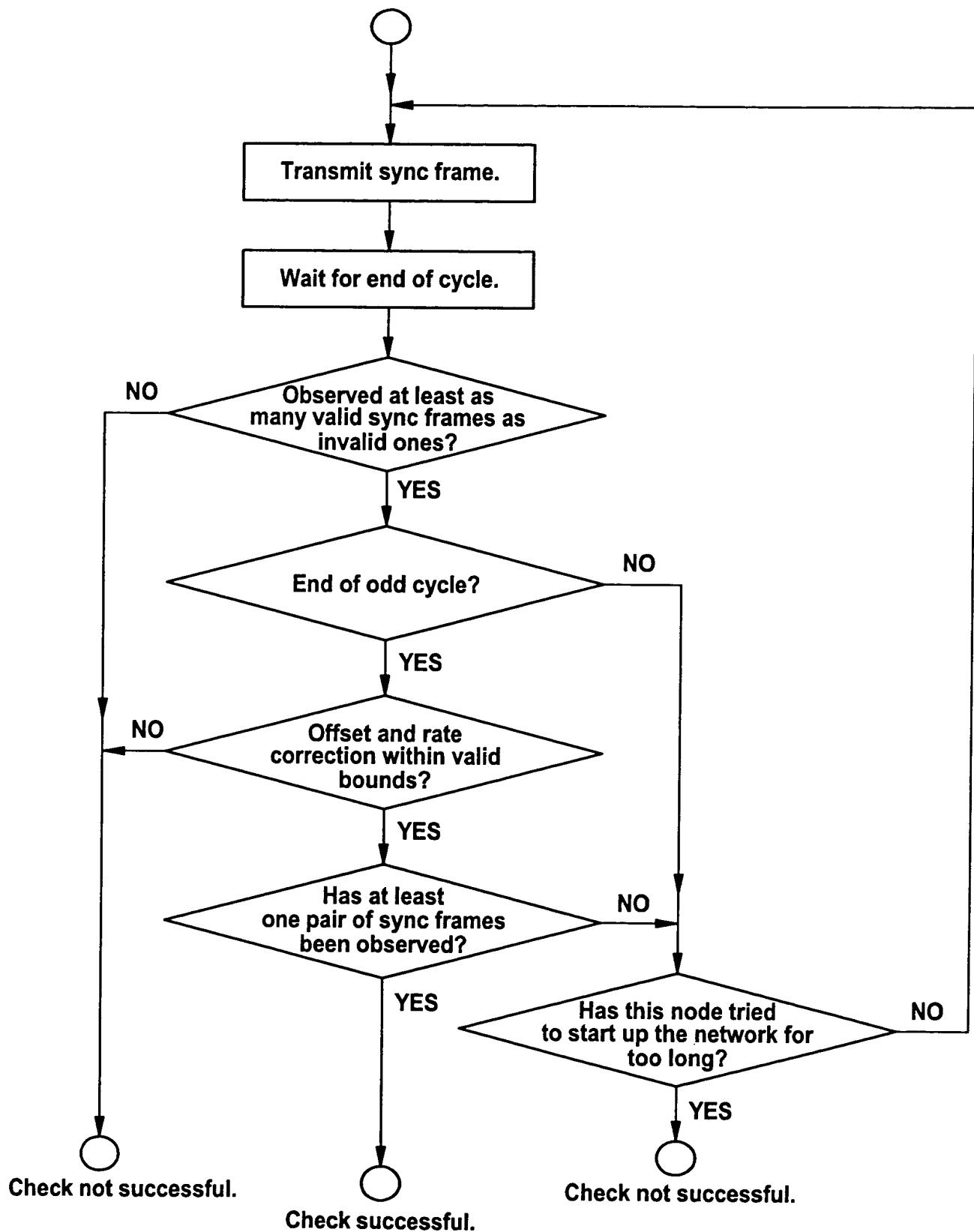


Fig. 54

Initial Synchronization

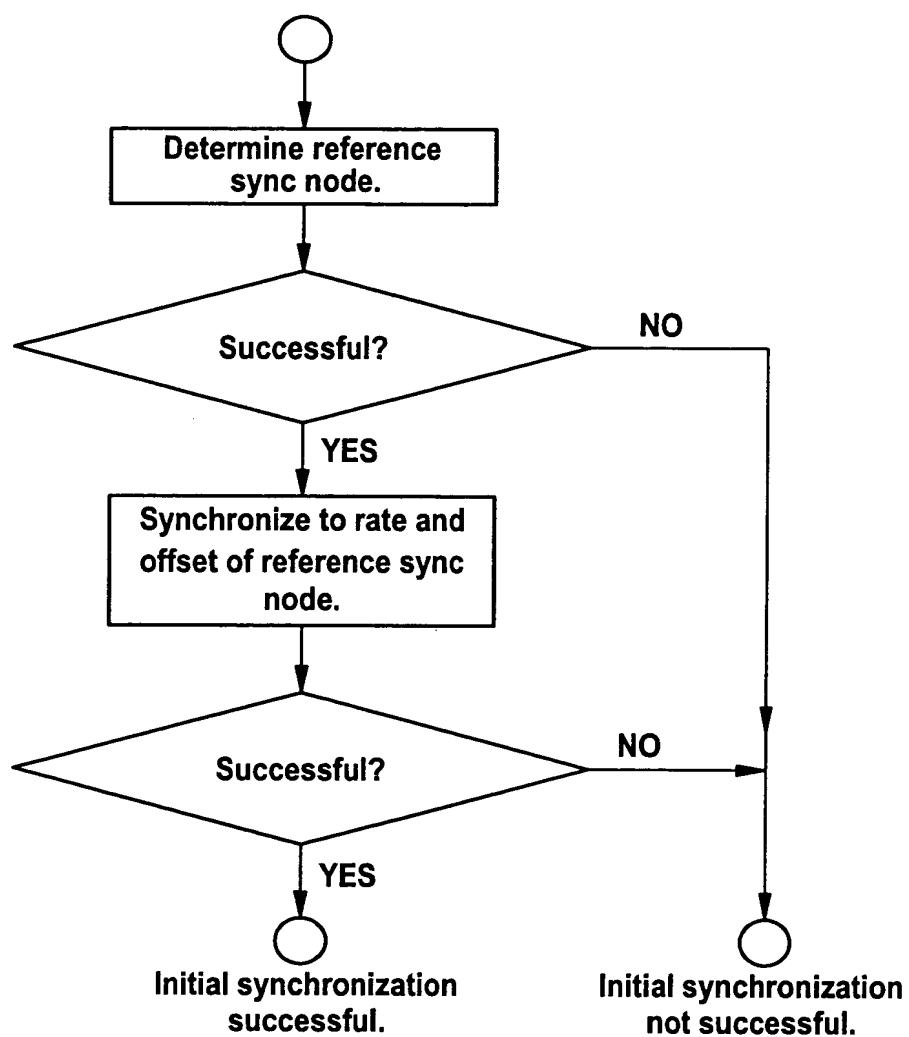


Fig. 55

Check on successful integration

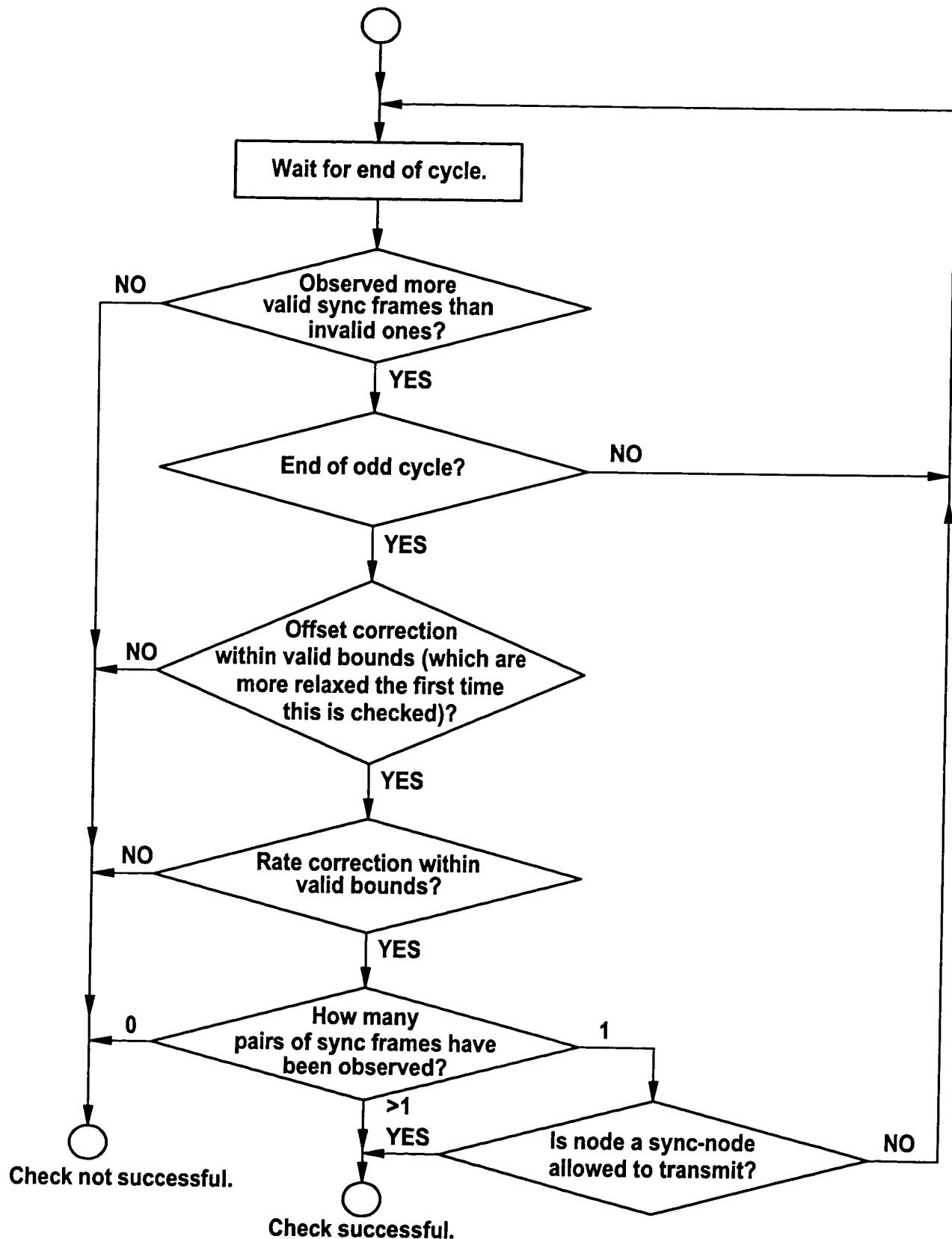


Fig. 56

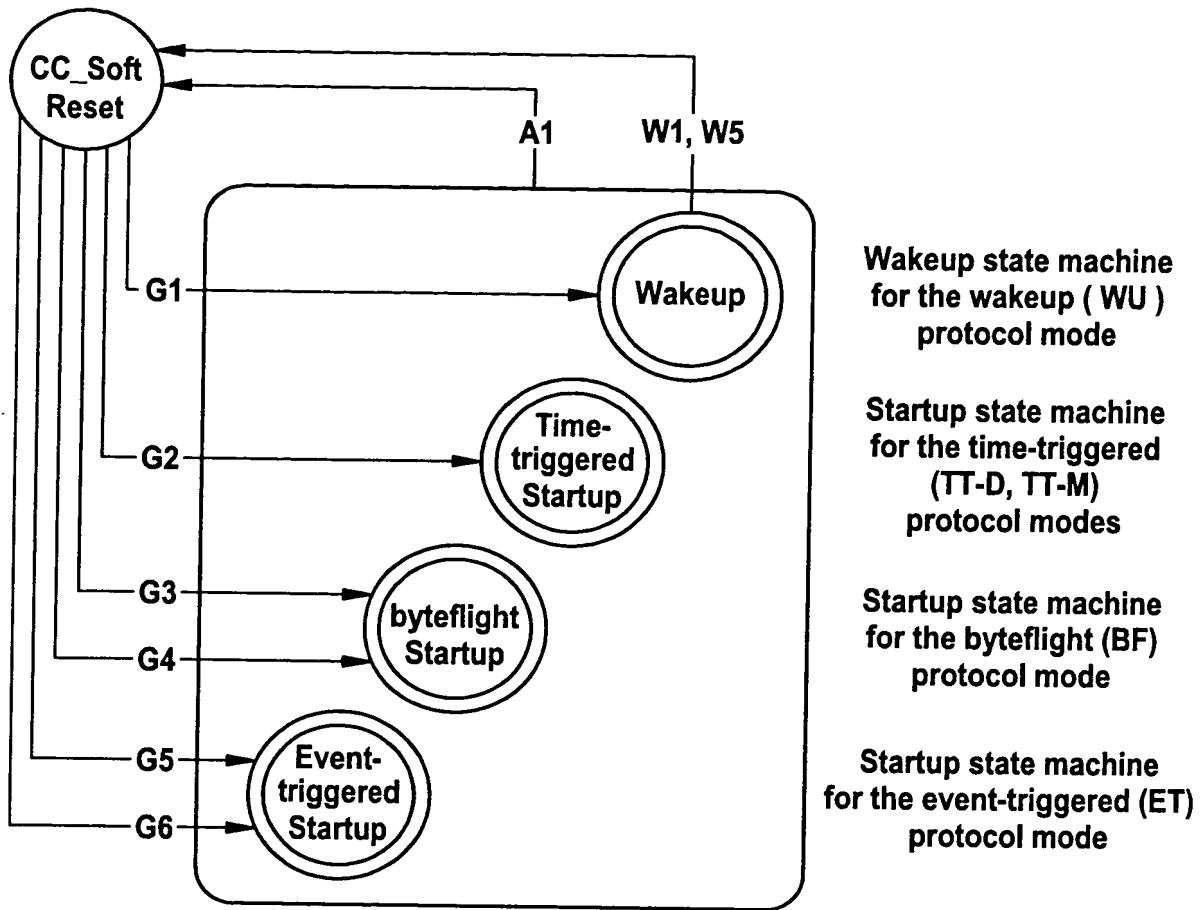


Fig. 57

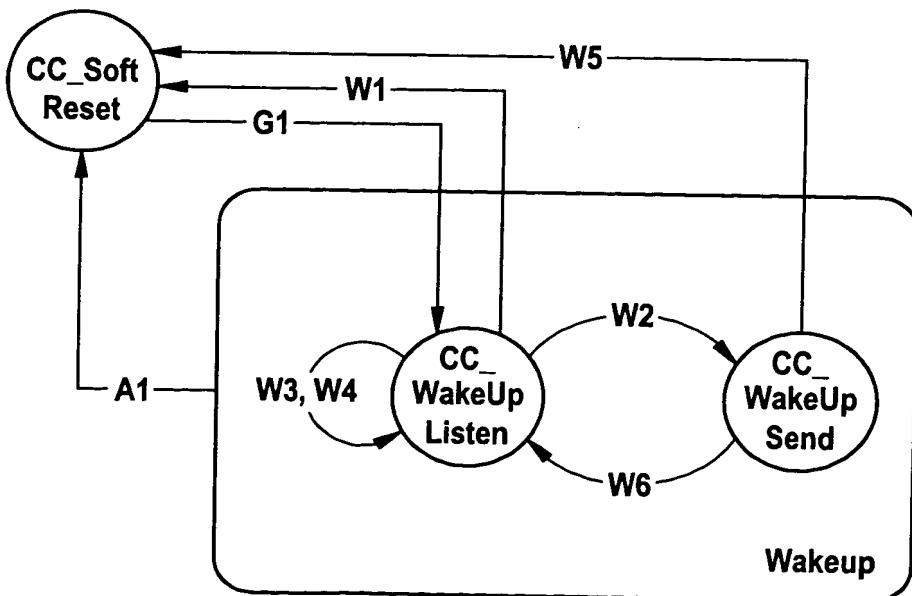


Fig. 58

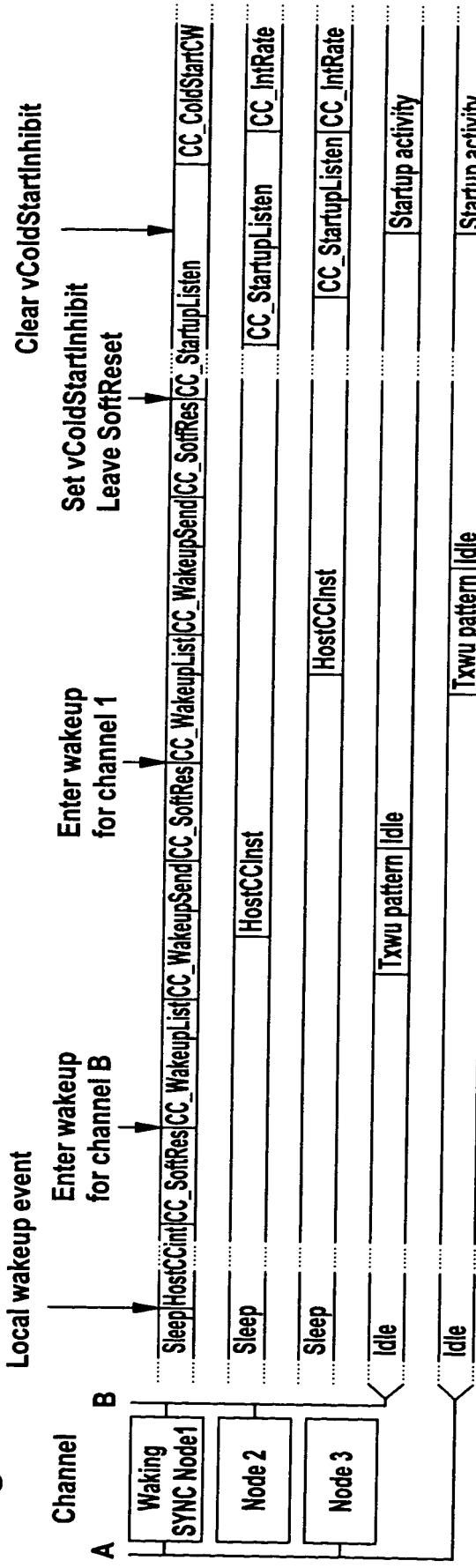


Fig. 59

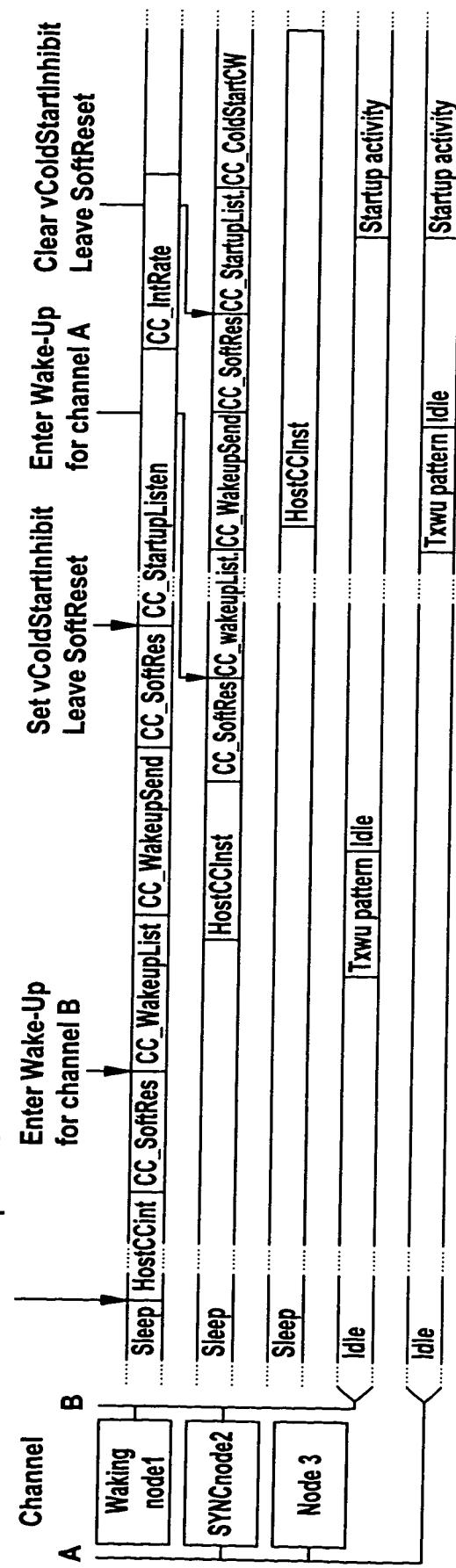


Fig. 60

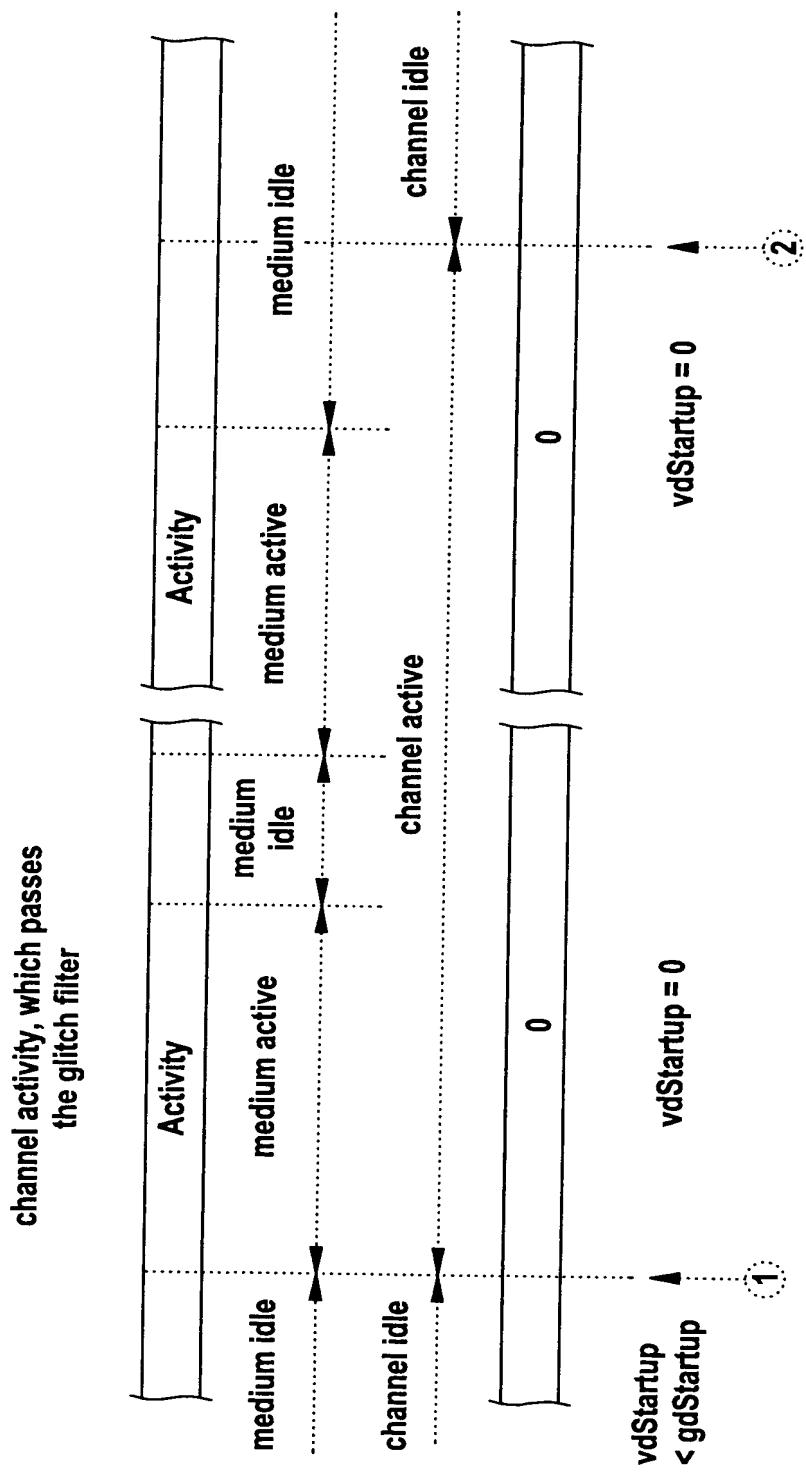


Fig. 61

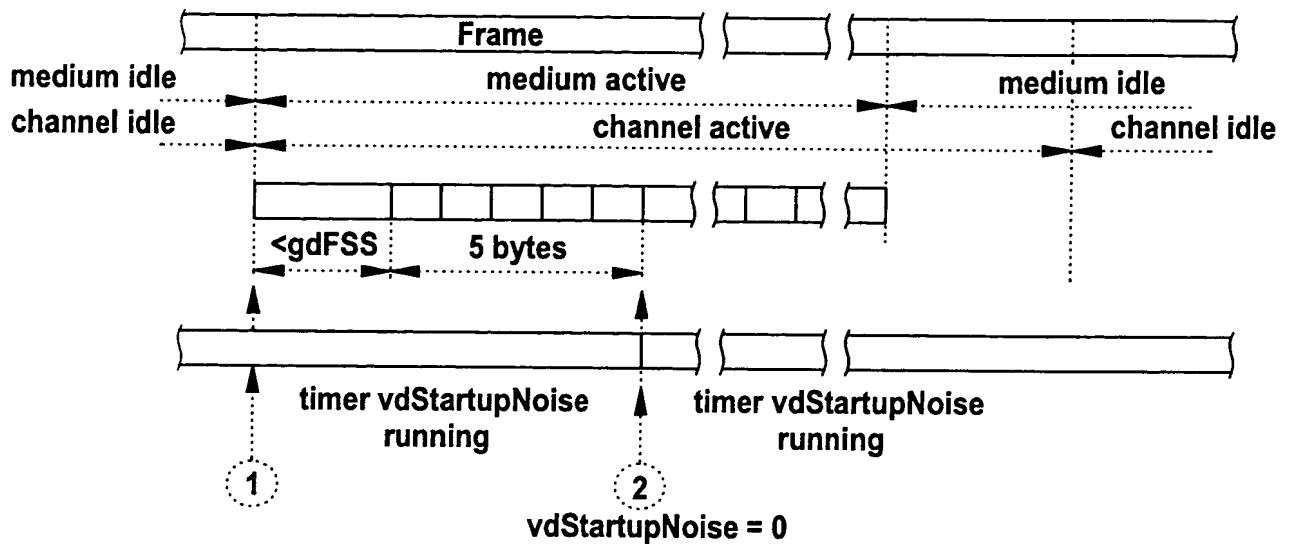


Fig. 62

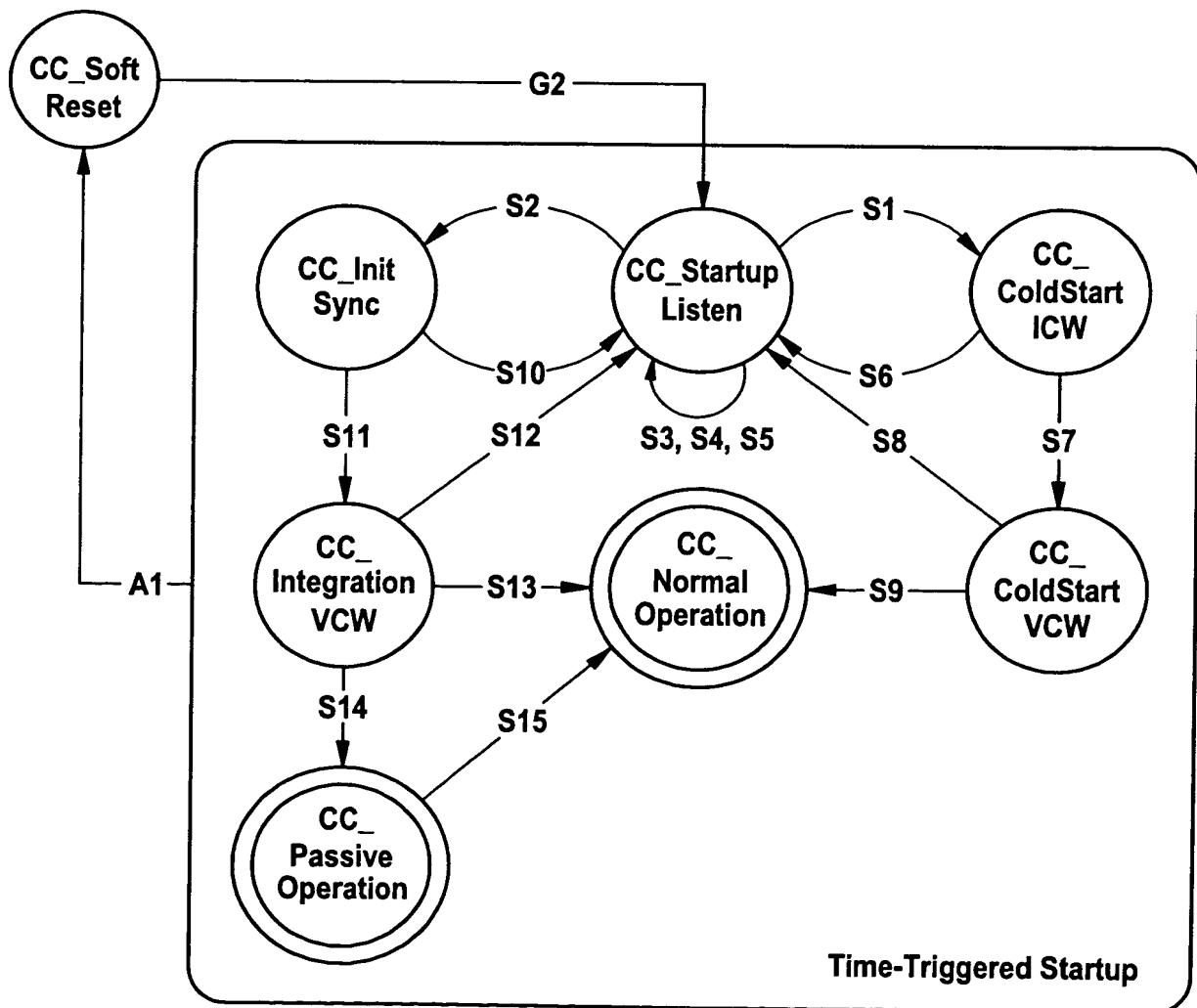


Fig. 63

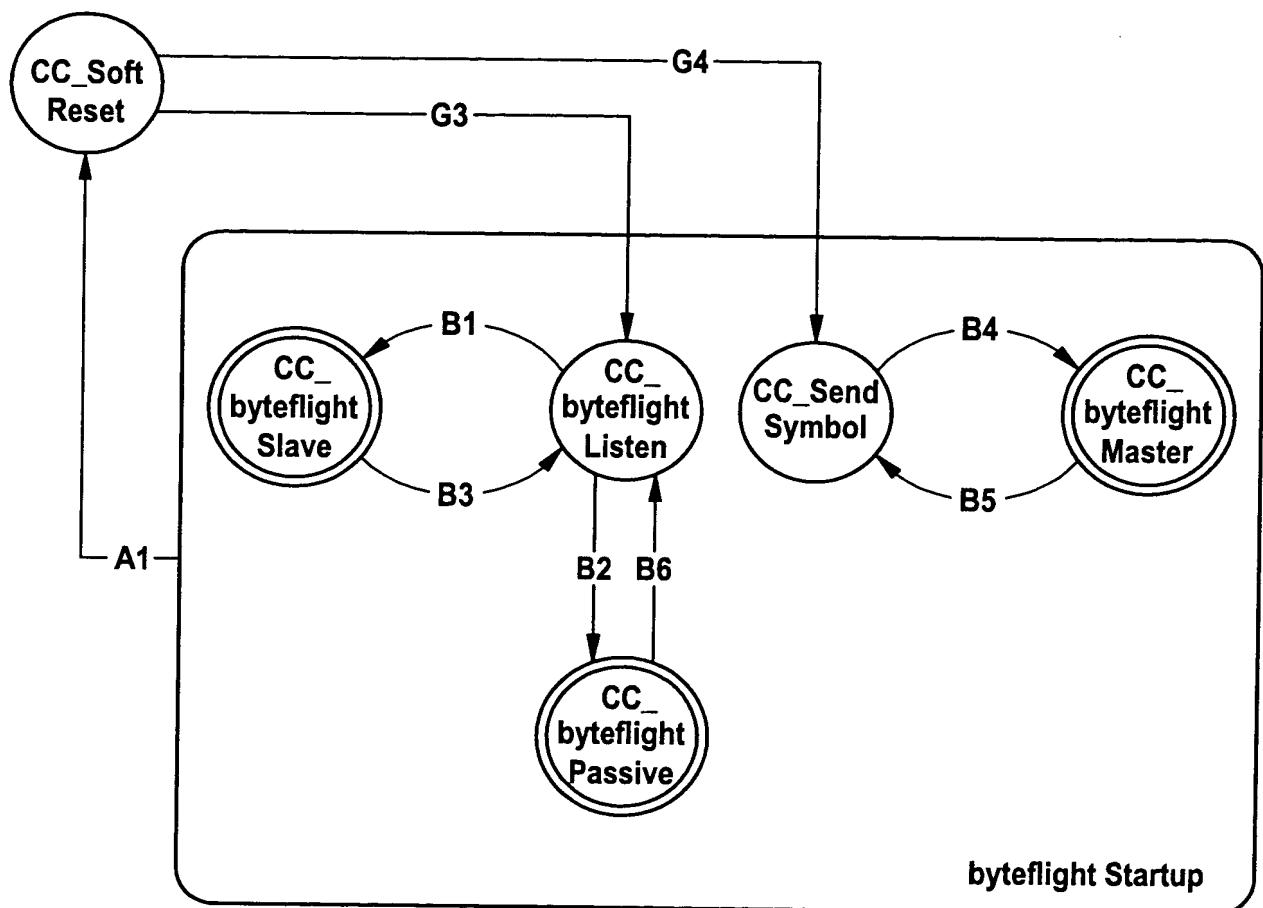


Fig. 64

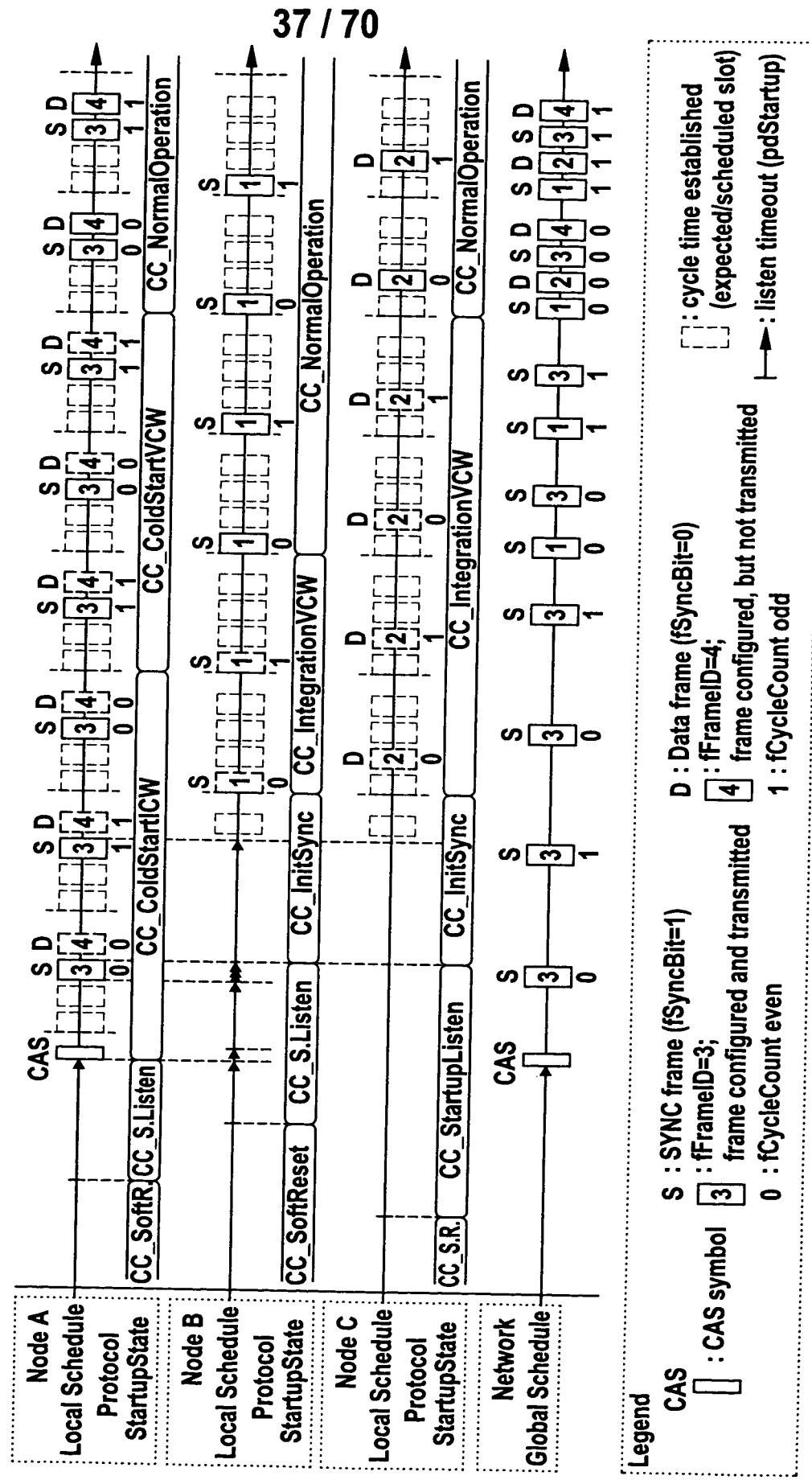


Fig. 65

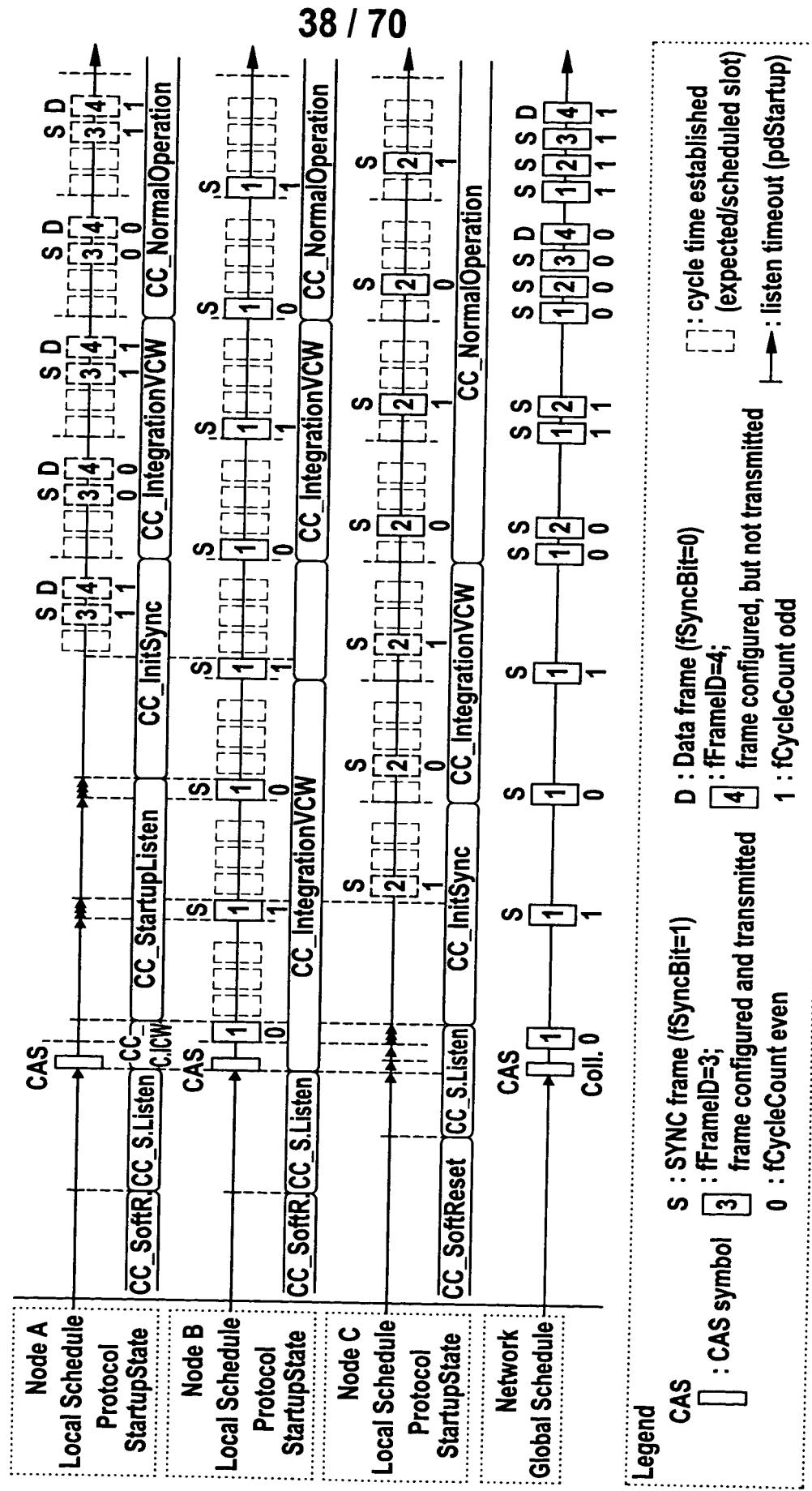


Fig. 66

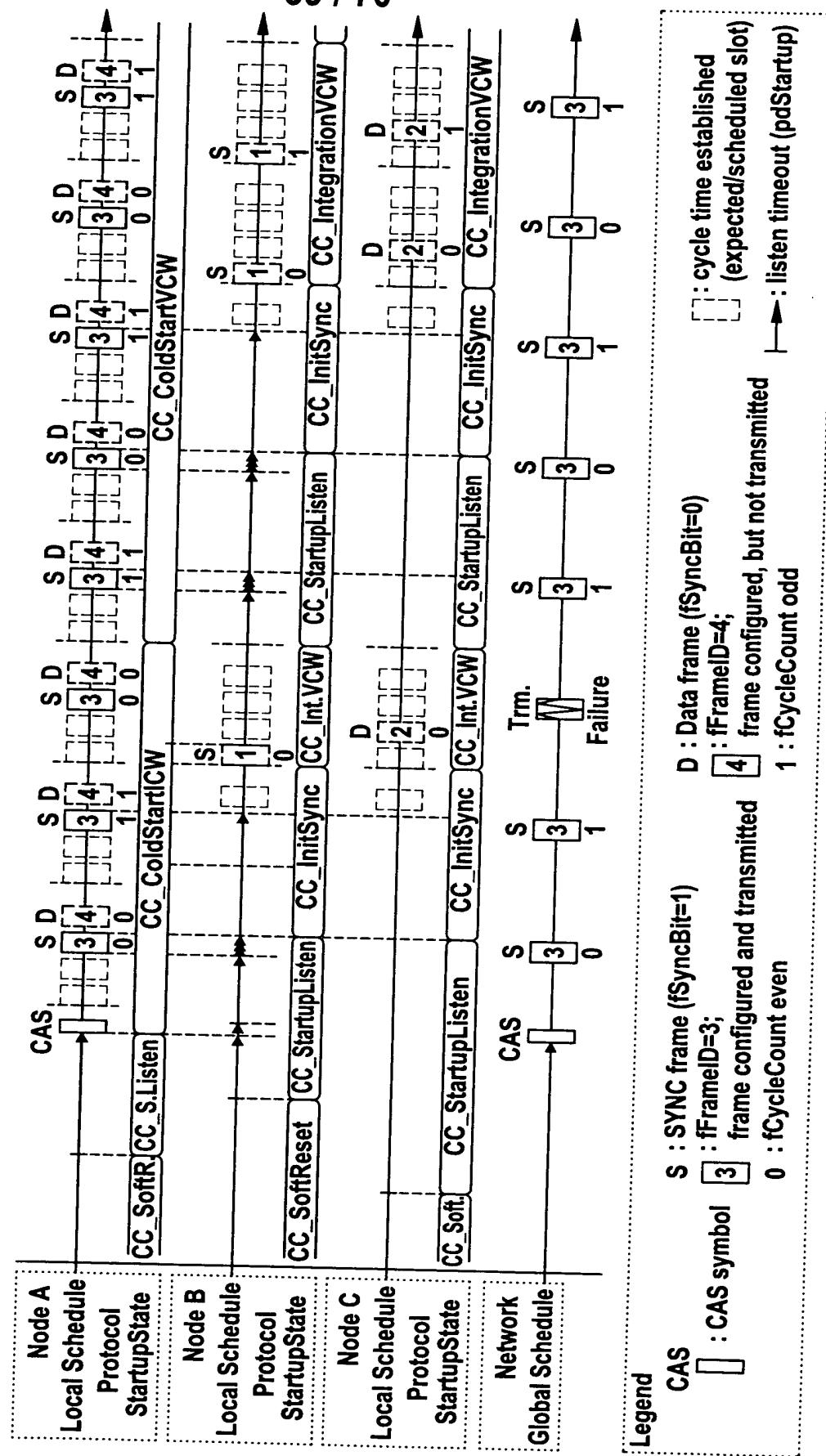


Fig. 67

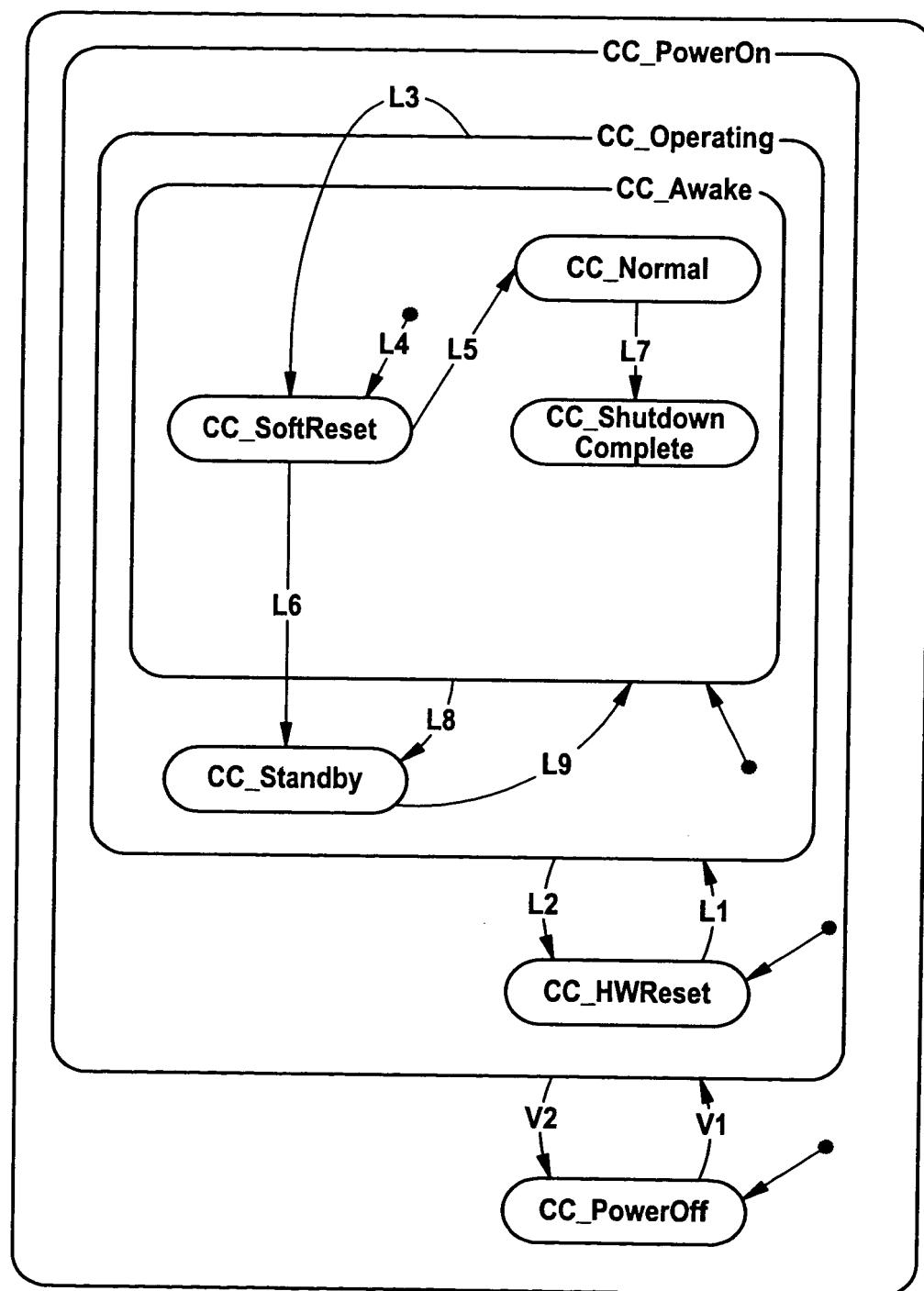


Fig. 68

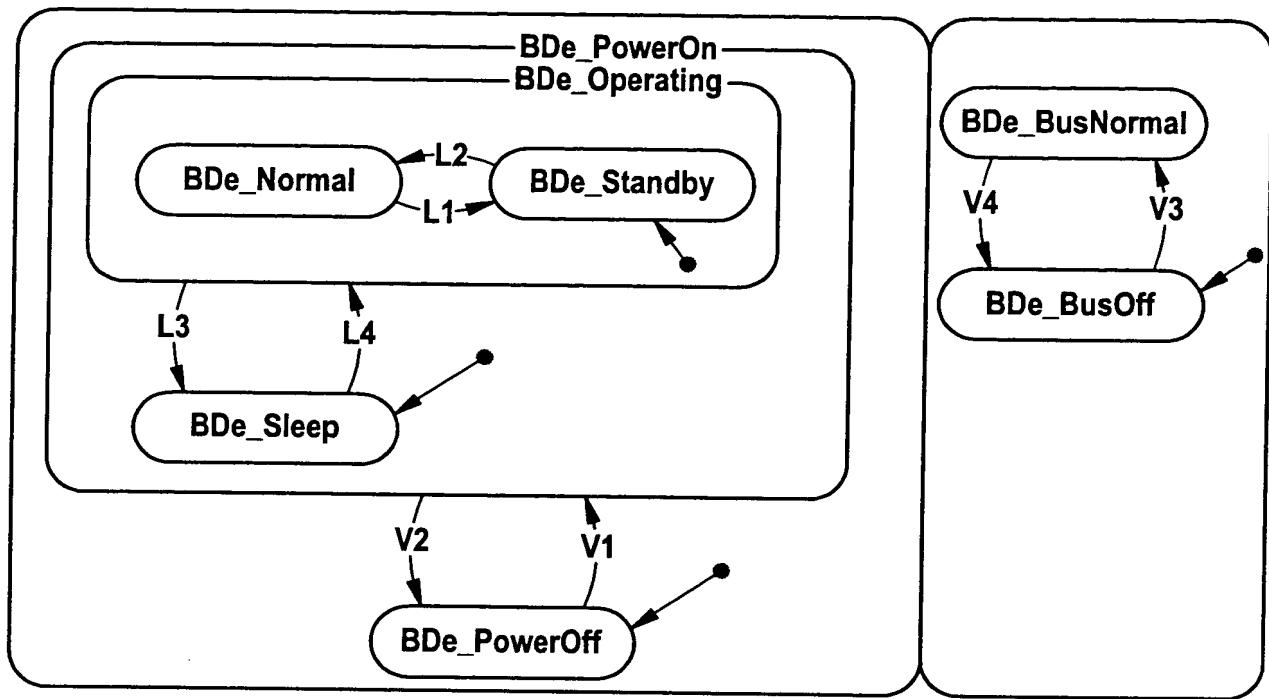


Fig. 69

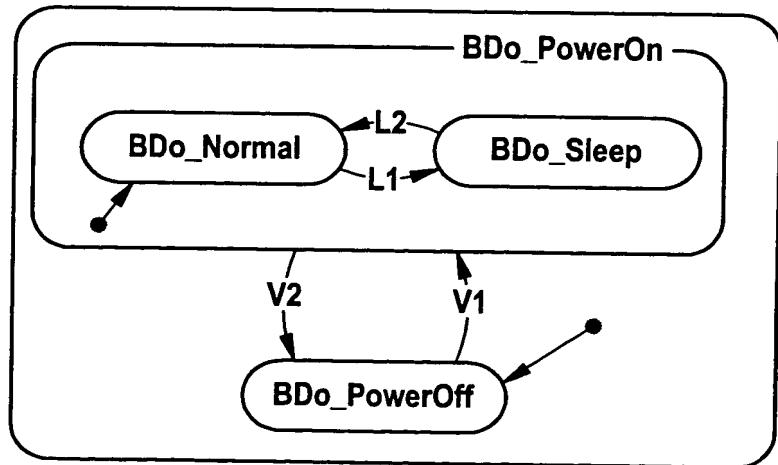


Fig. 70

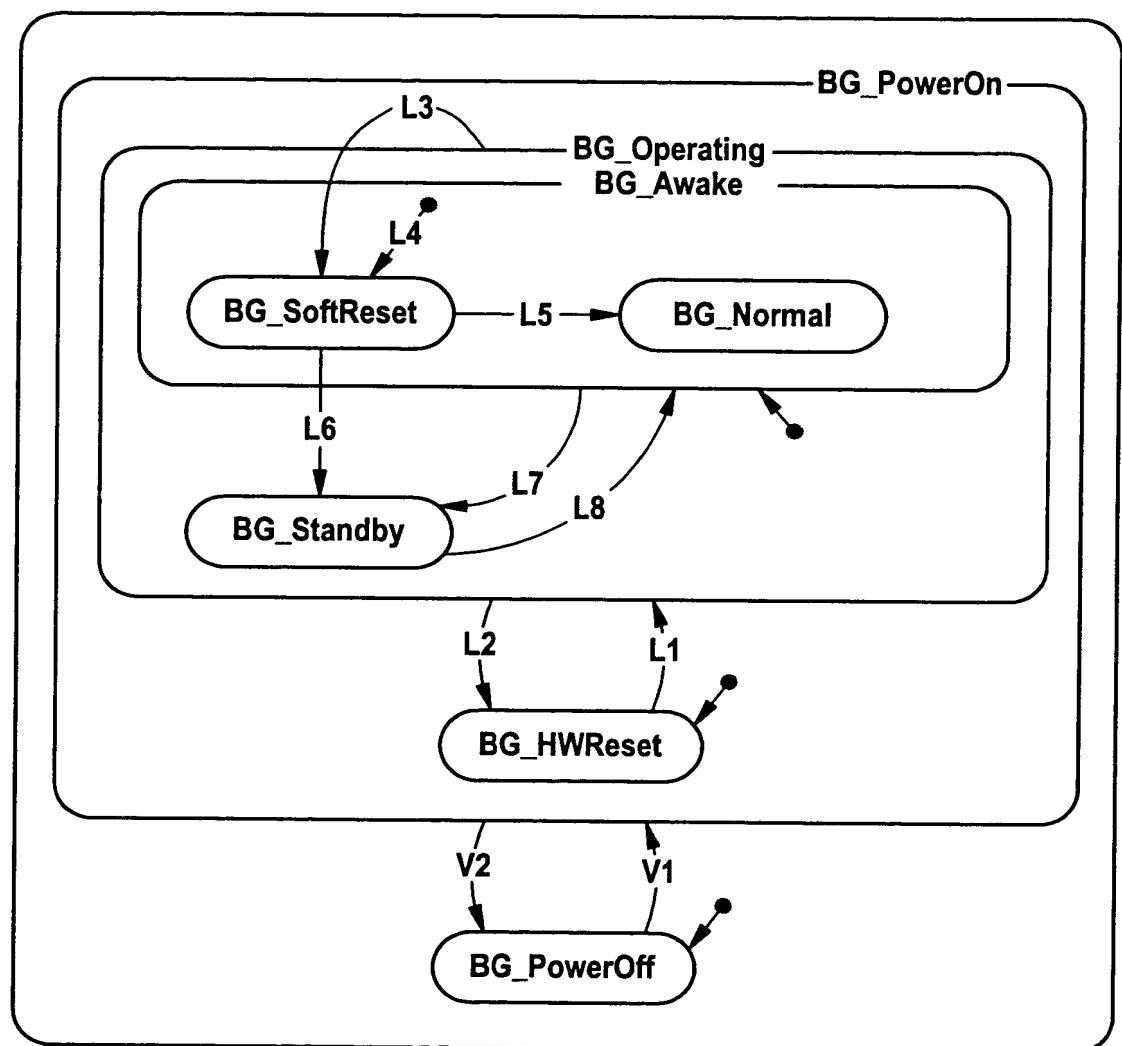


Fig. 71

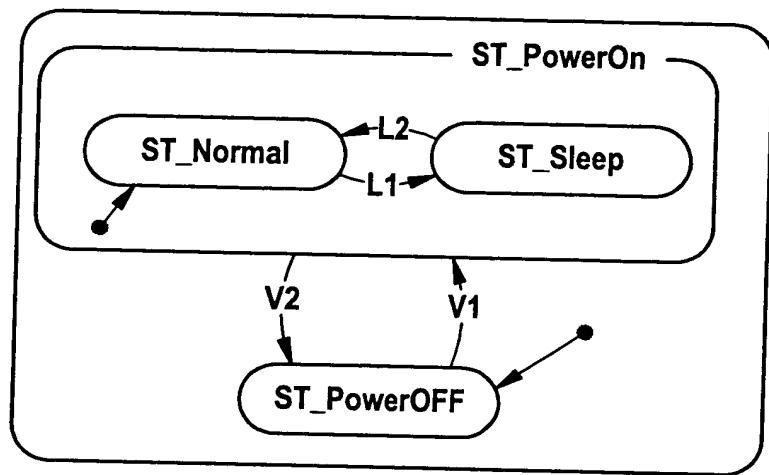


Fig. 72

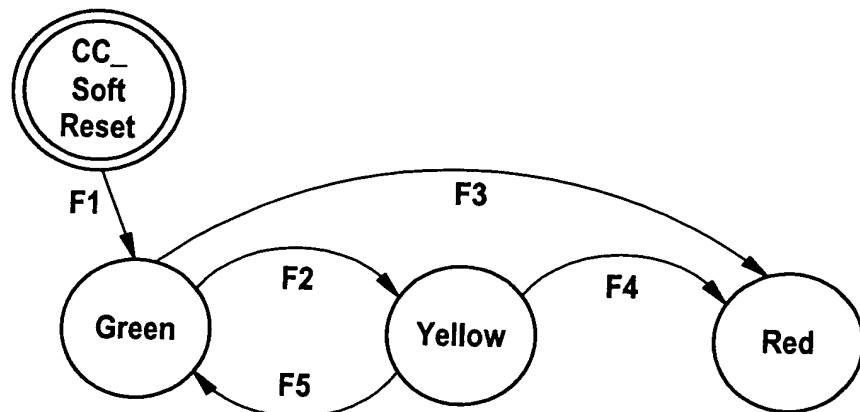


Fig. 73

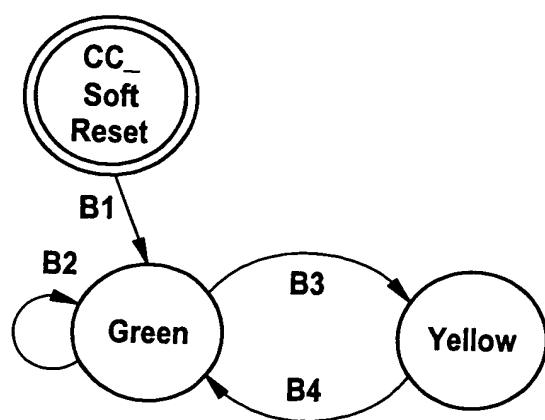


Fig. 74

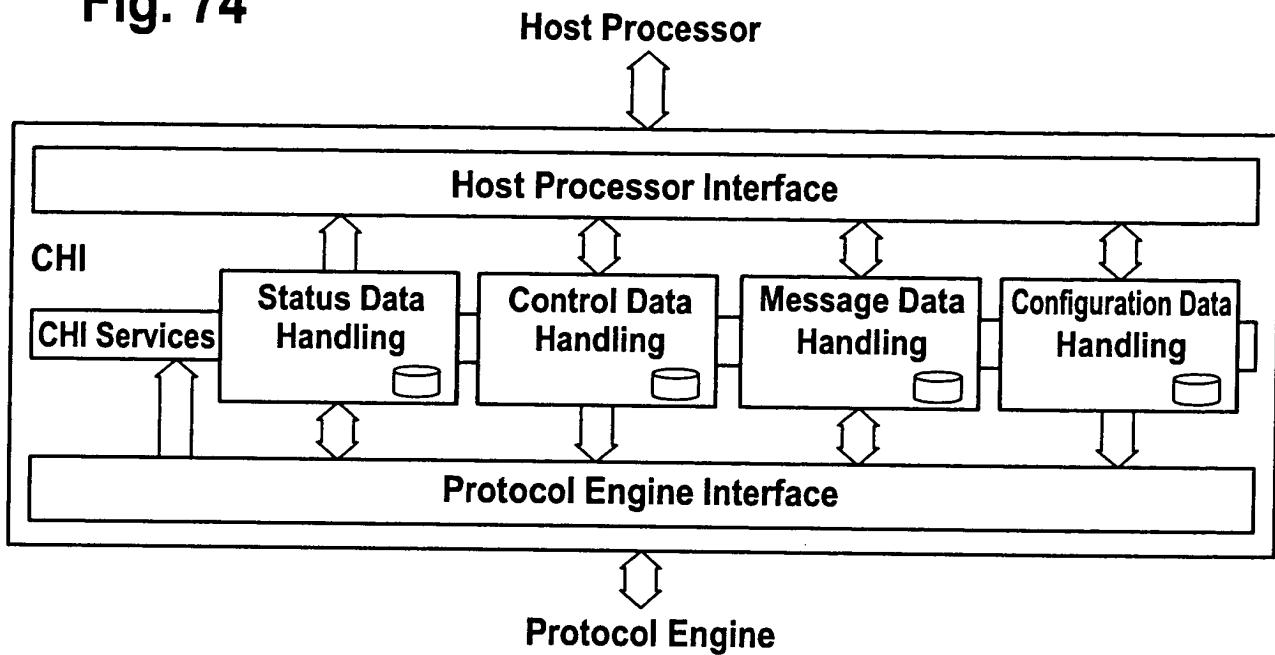


Fig. 75

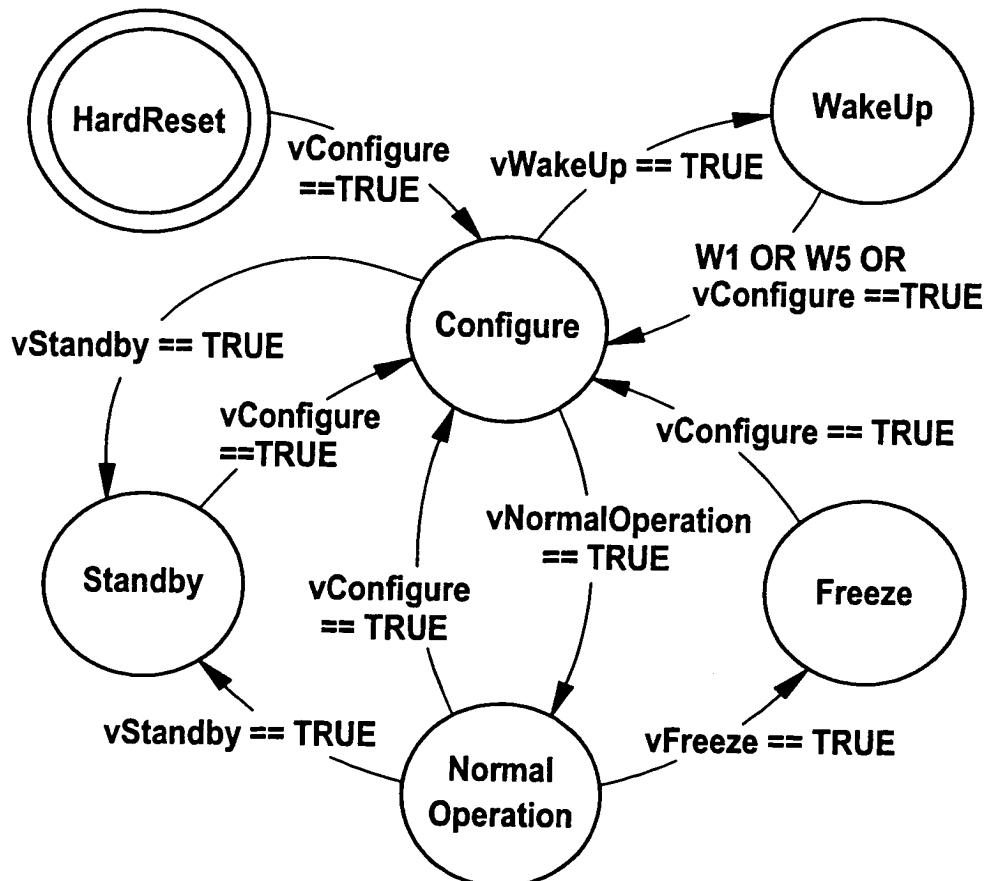


Fig. 76

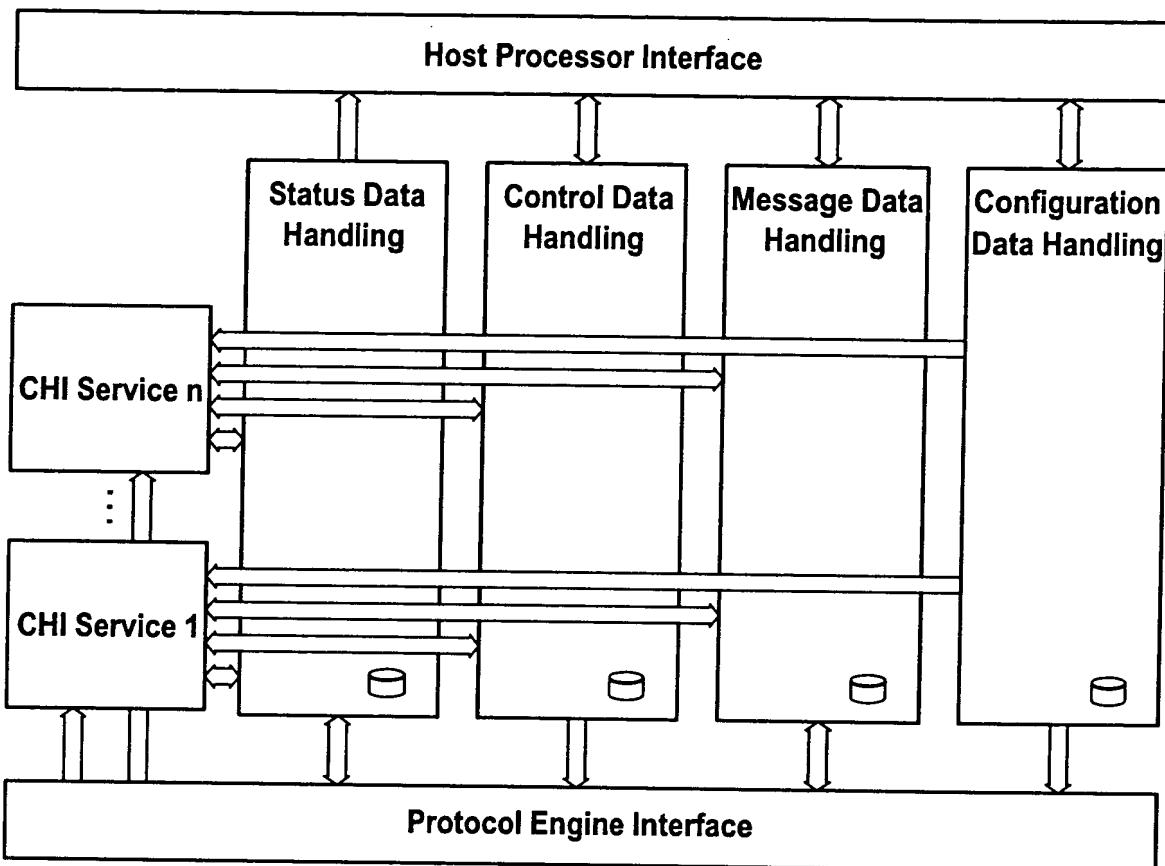


Fig. 77

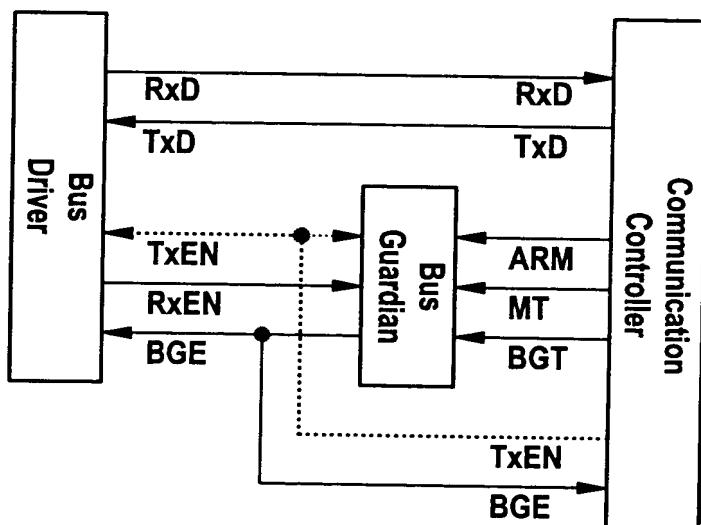


Fig. 78

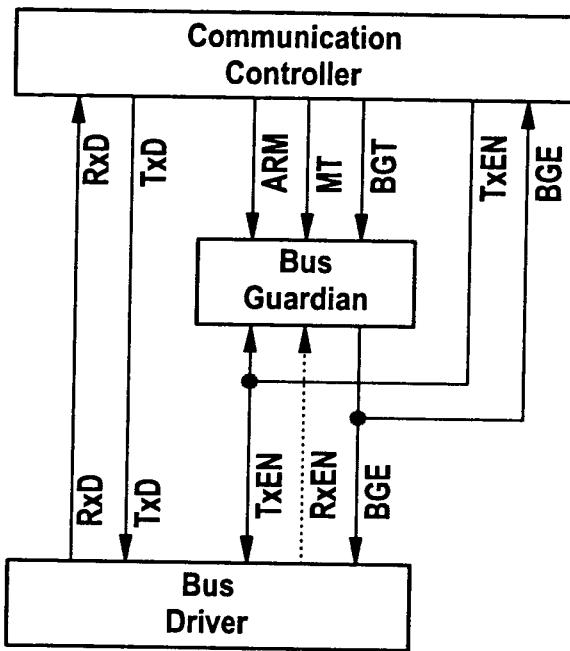


Fig. 79

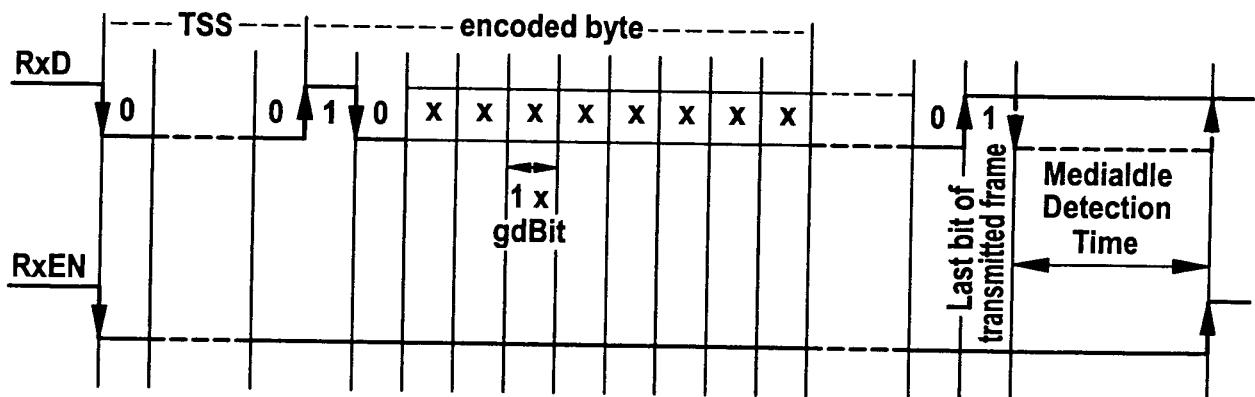


Fig. 80

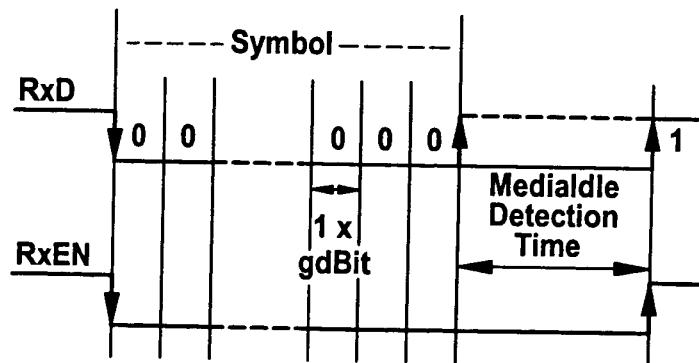


Fig. 81

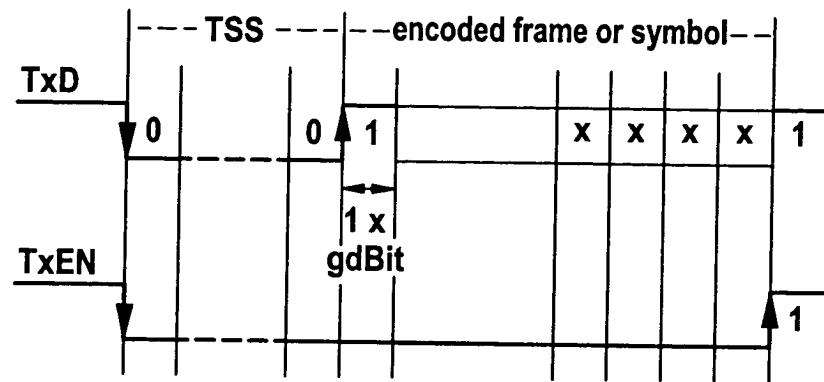
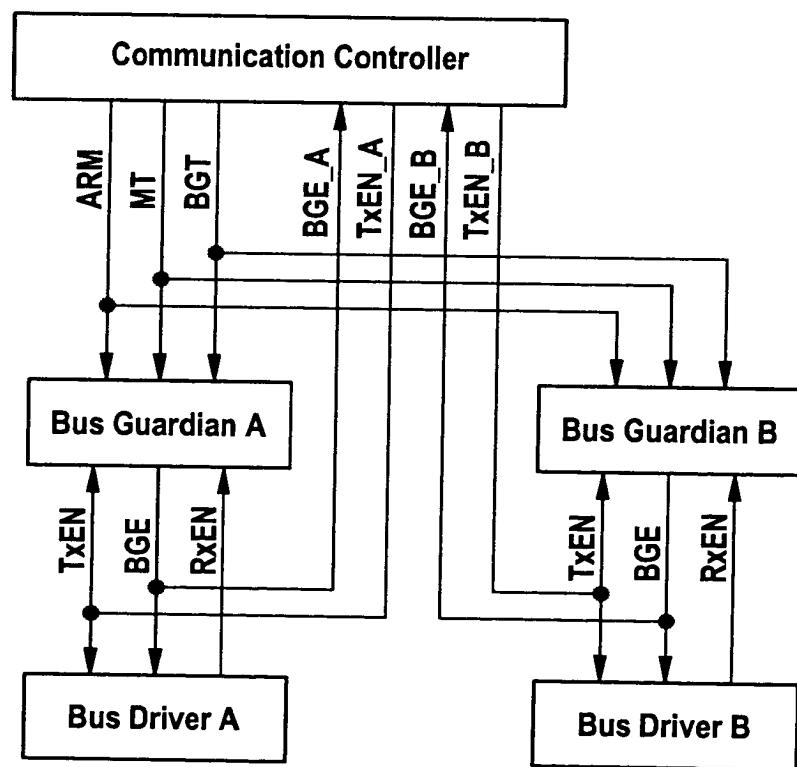


Fig. 82



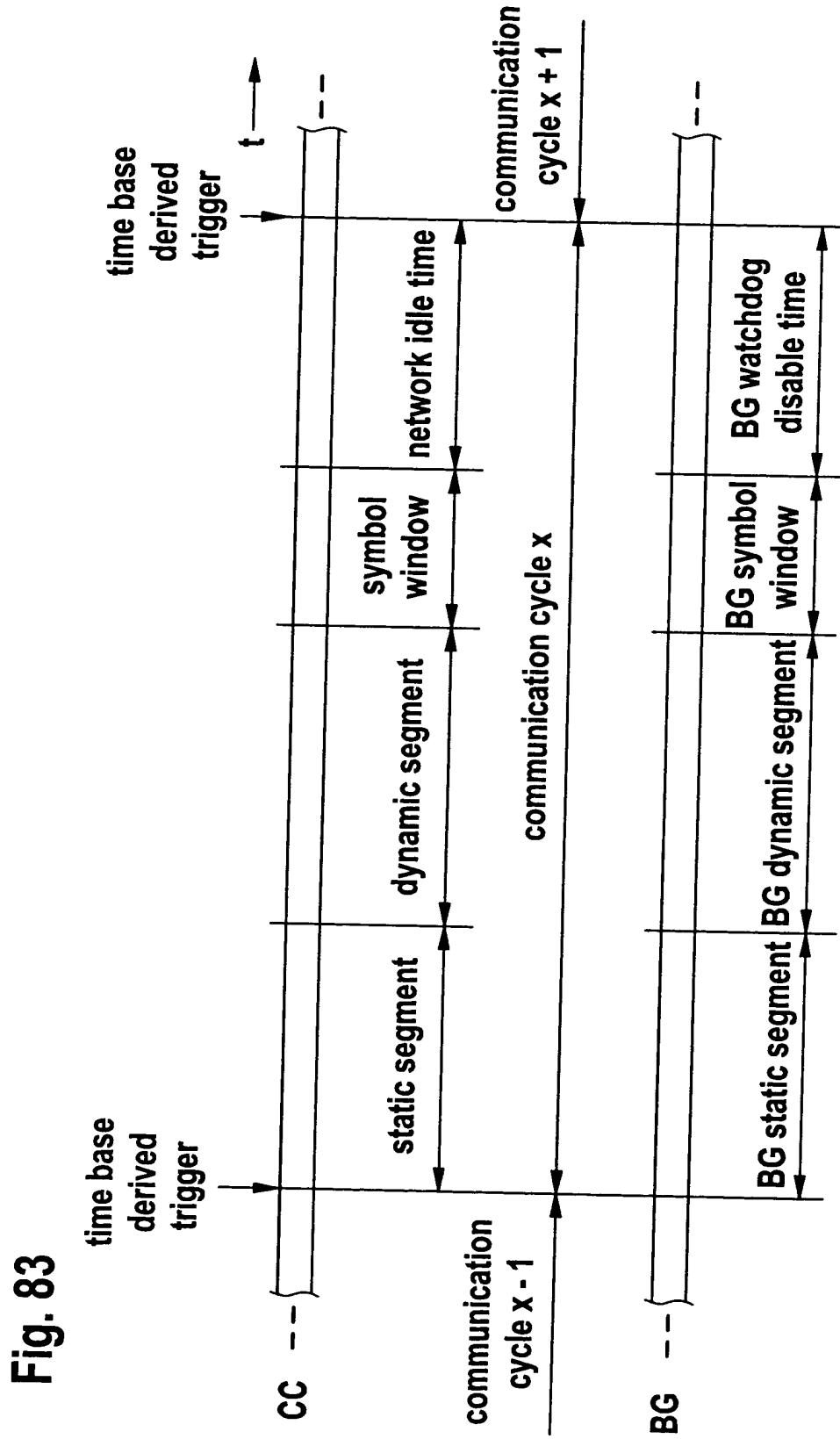


Fig. 83

Fig. 84

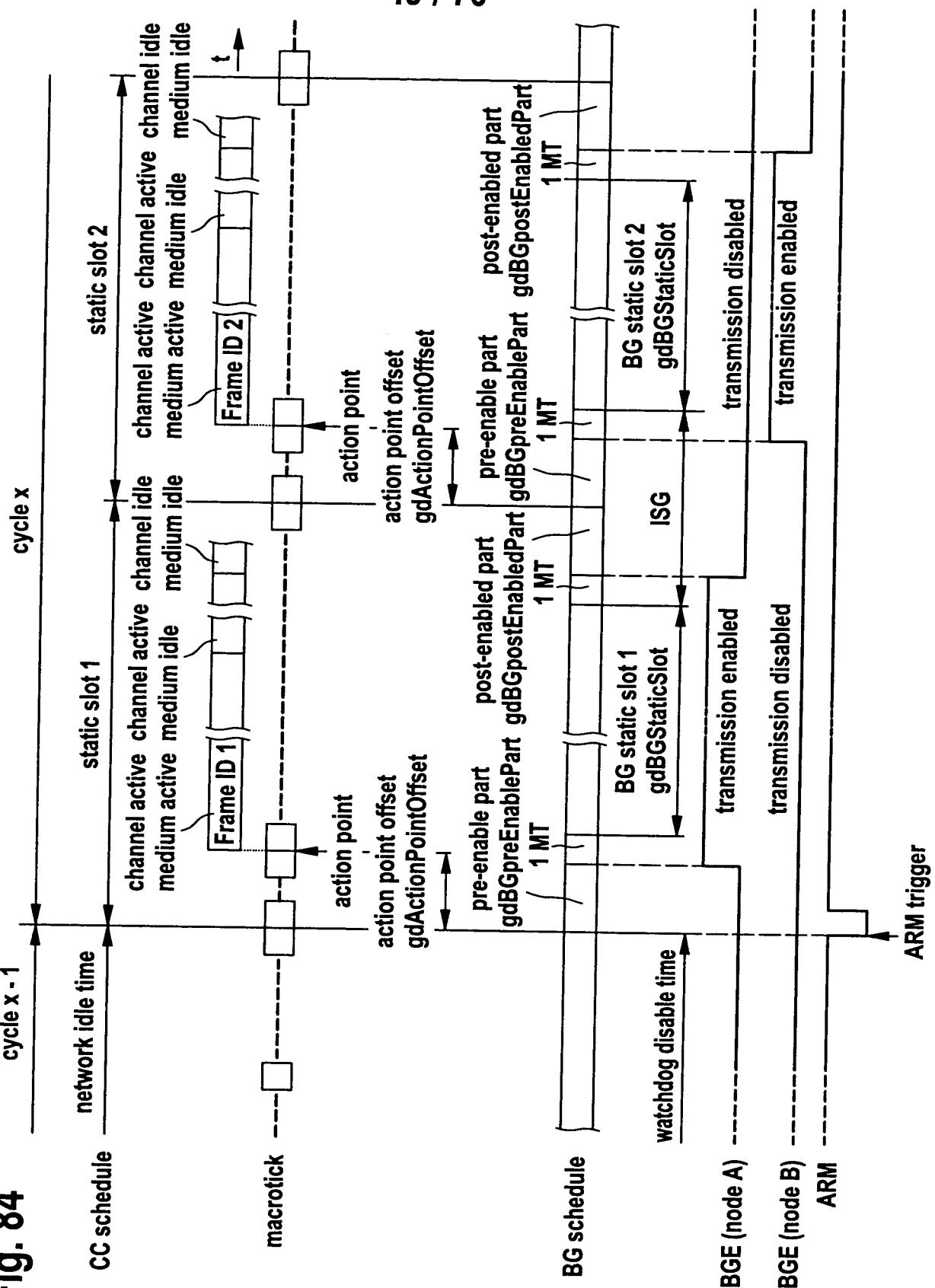


Fig. 85

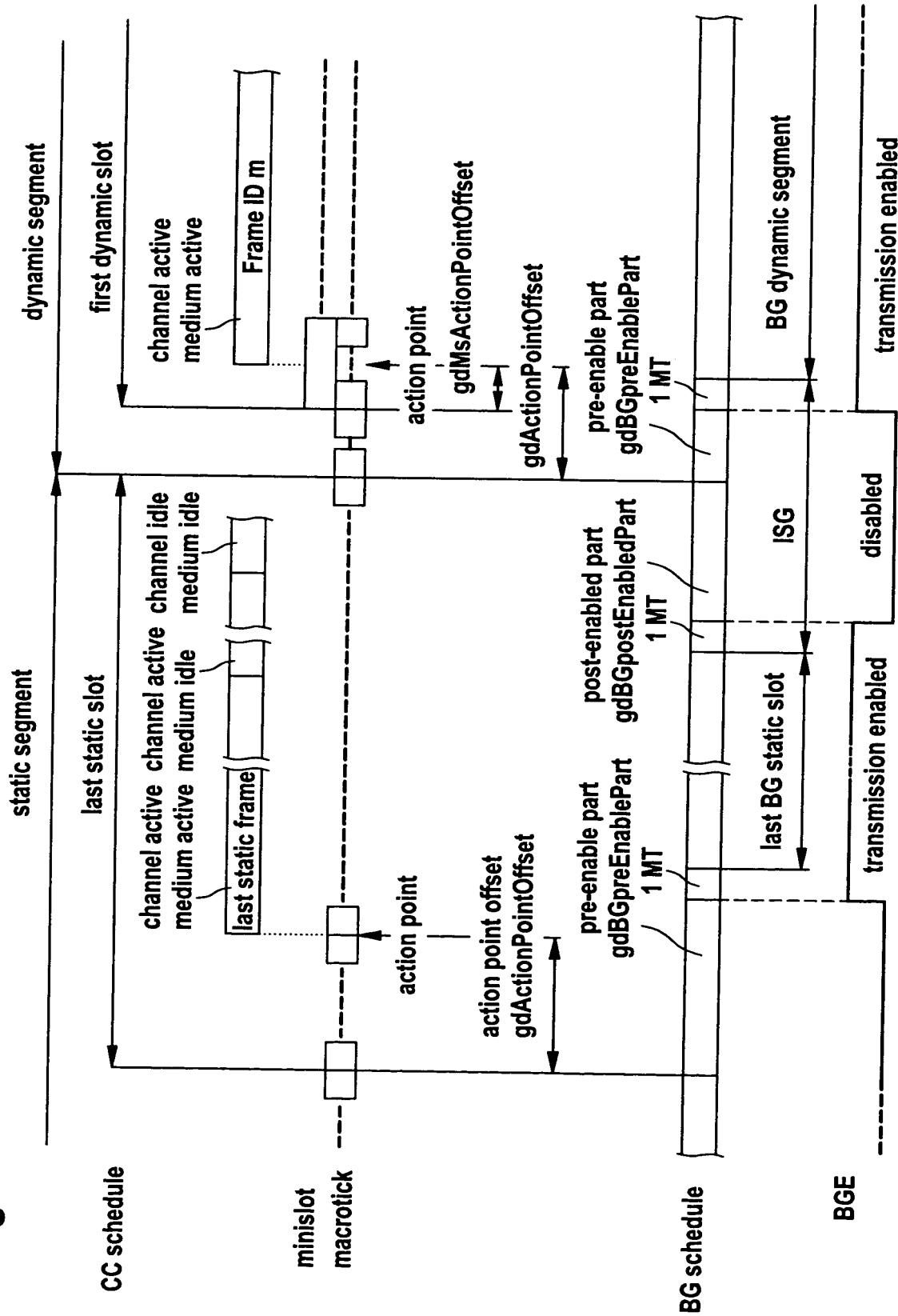


Fig. 86

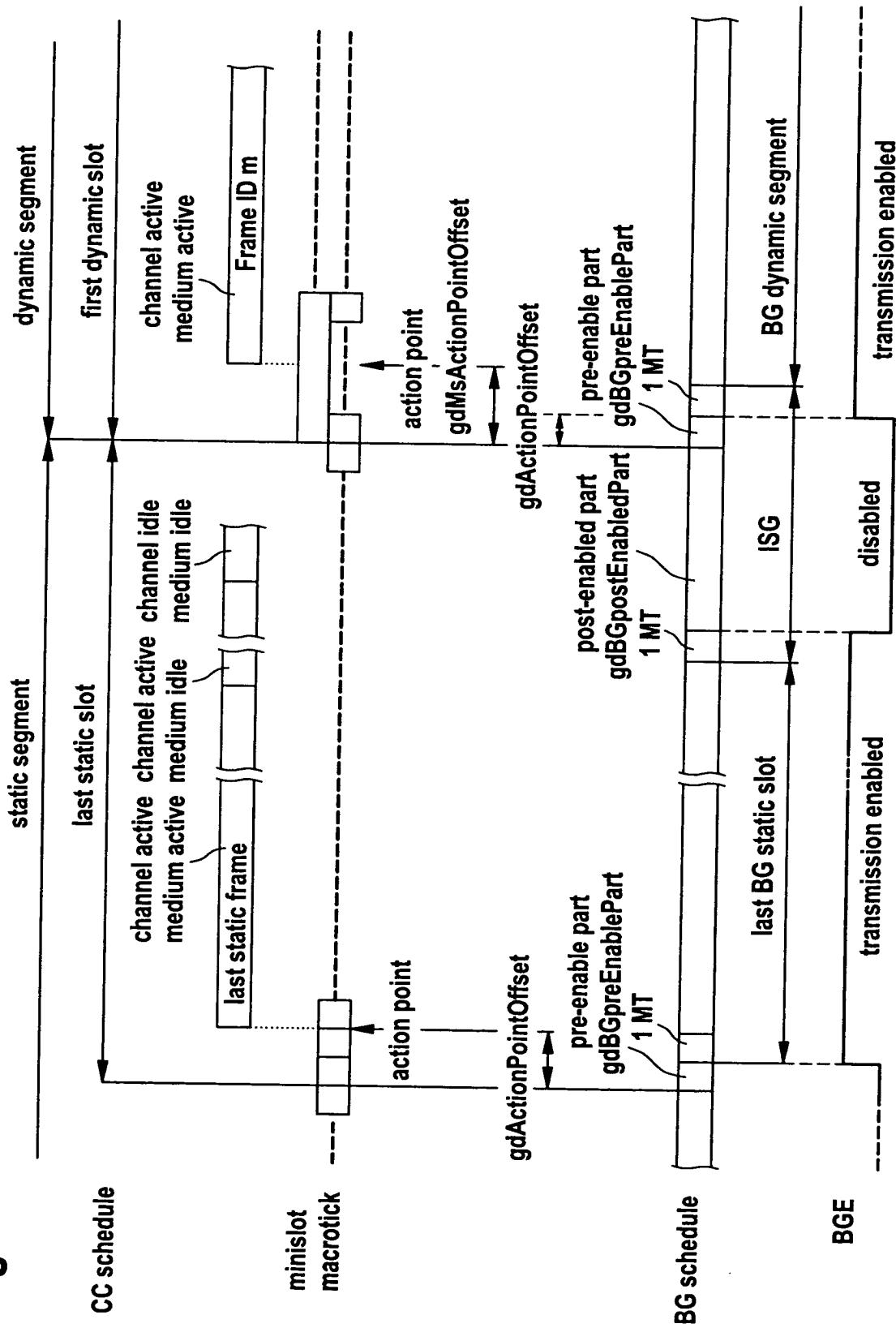


Fig. 87

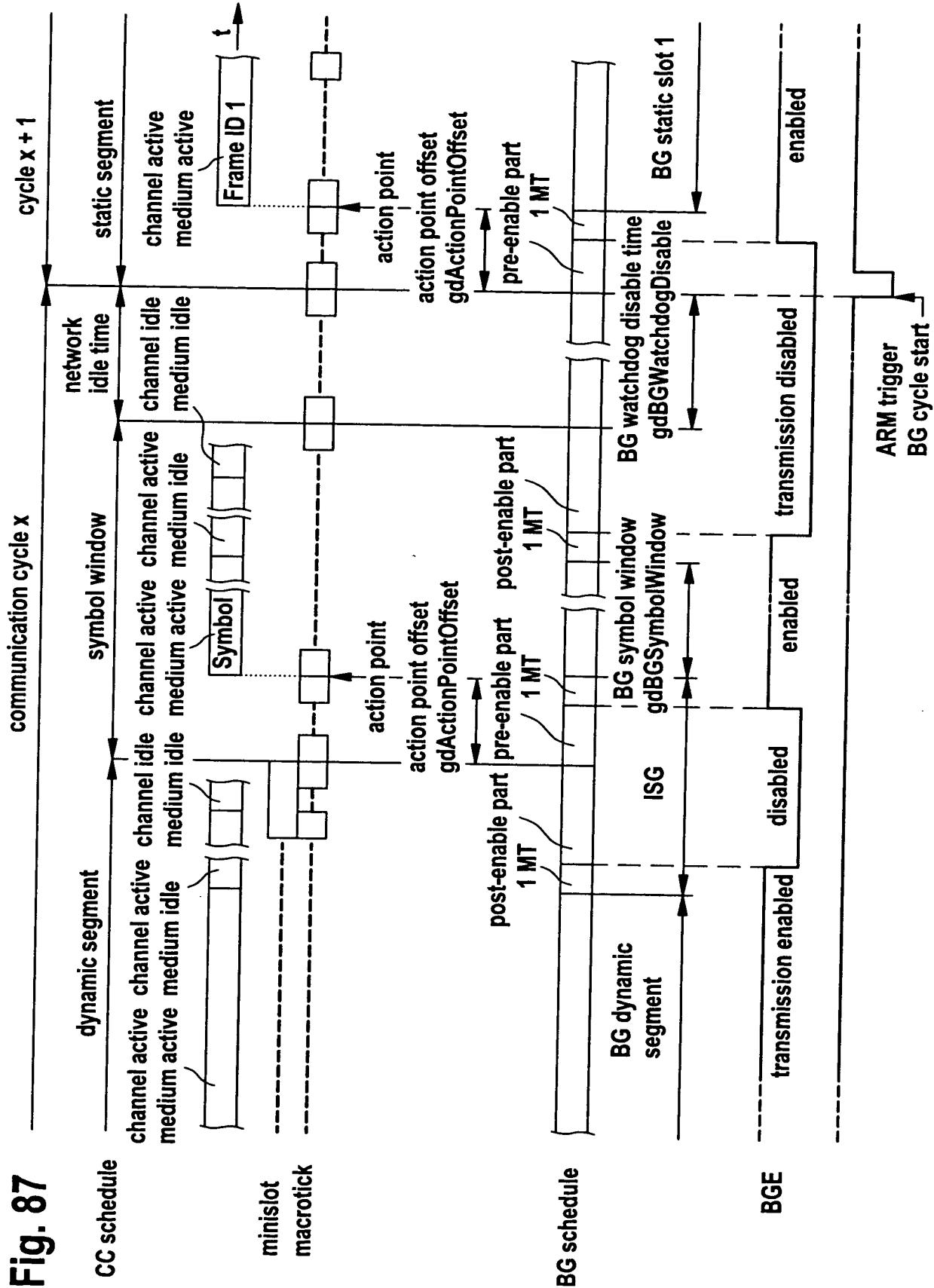
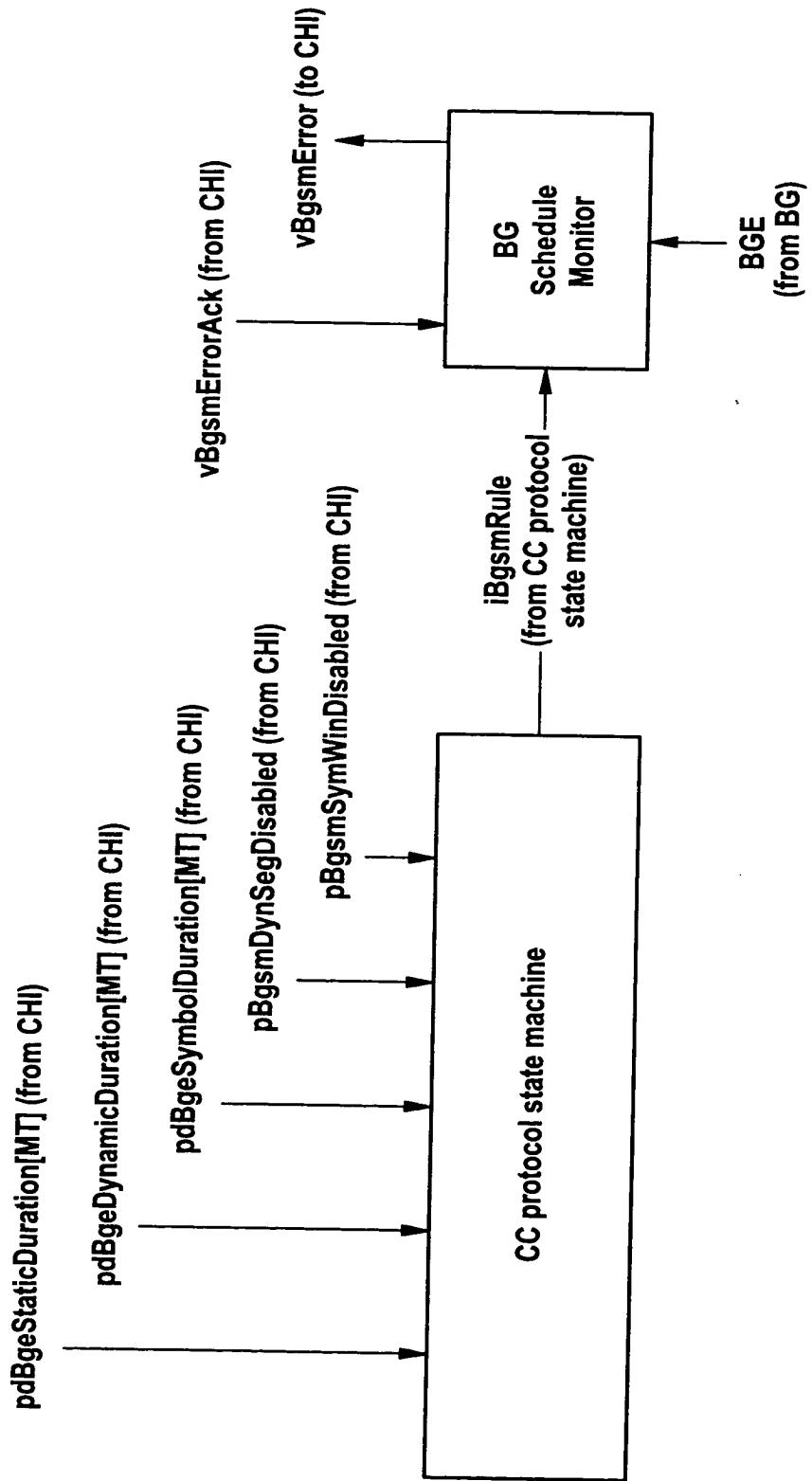


Fig. 88



iBgsmRule == BGE_X

Fig. 89

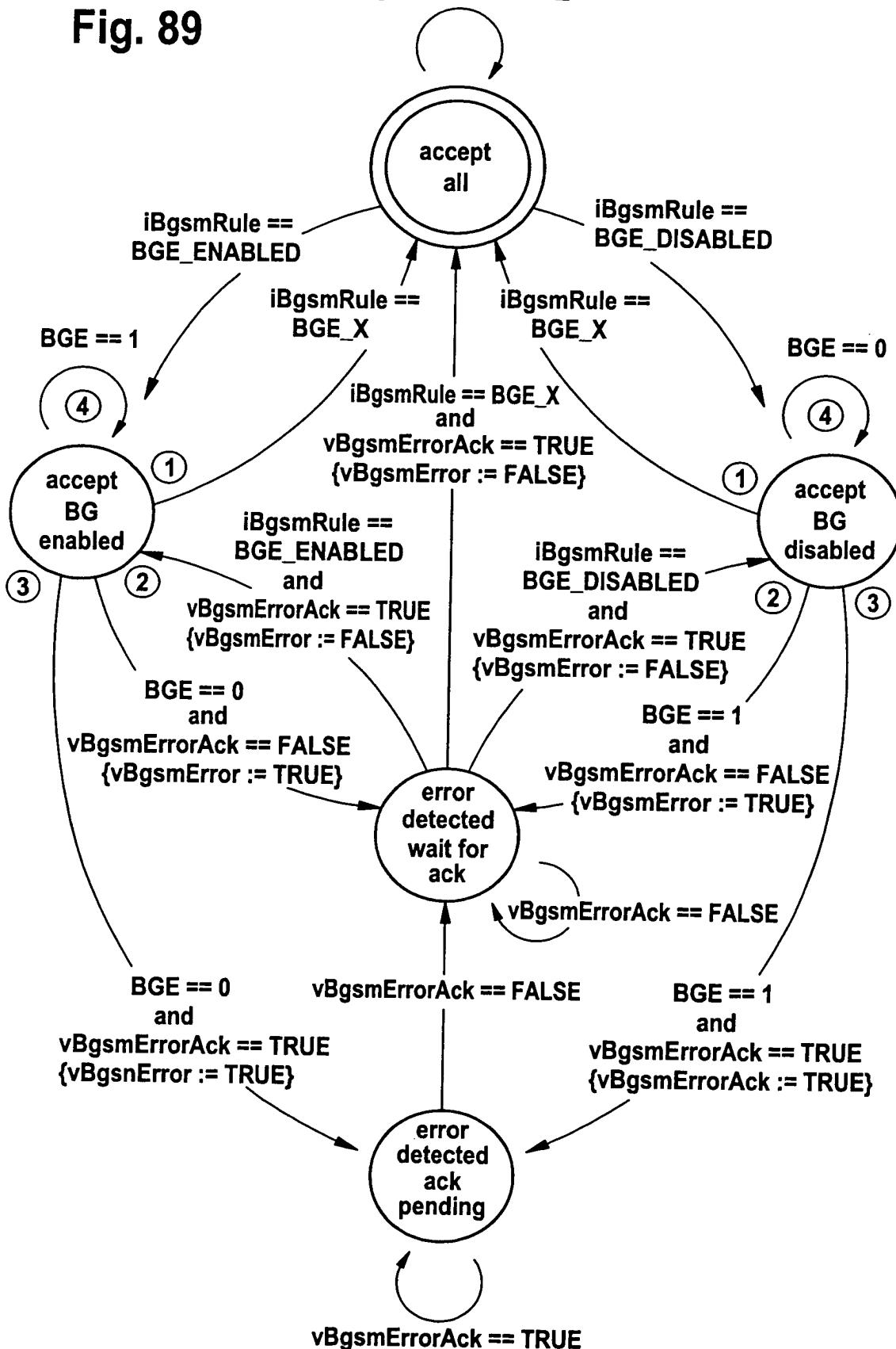


Fig. 90

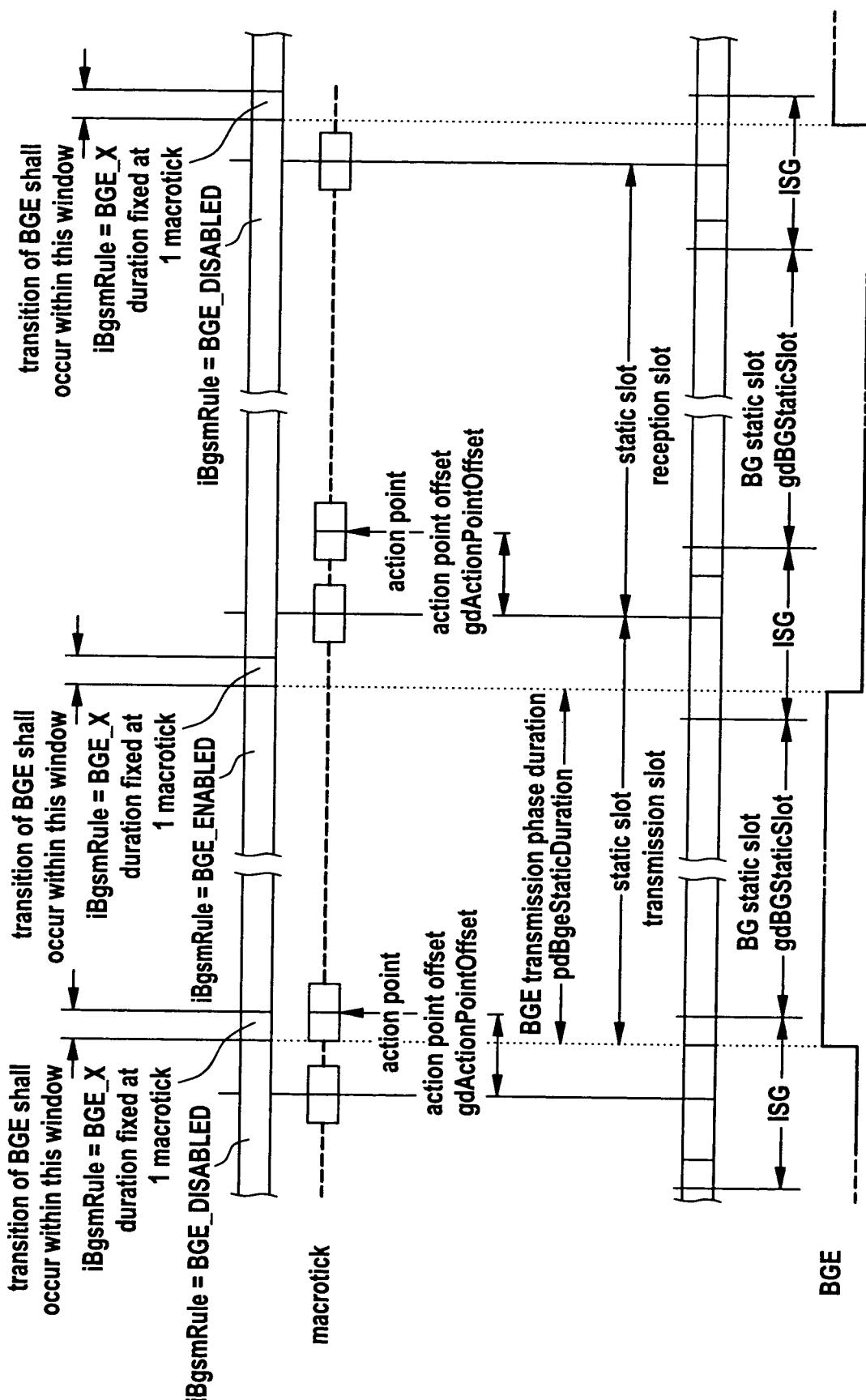


Fig. 91

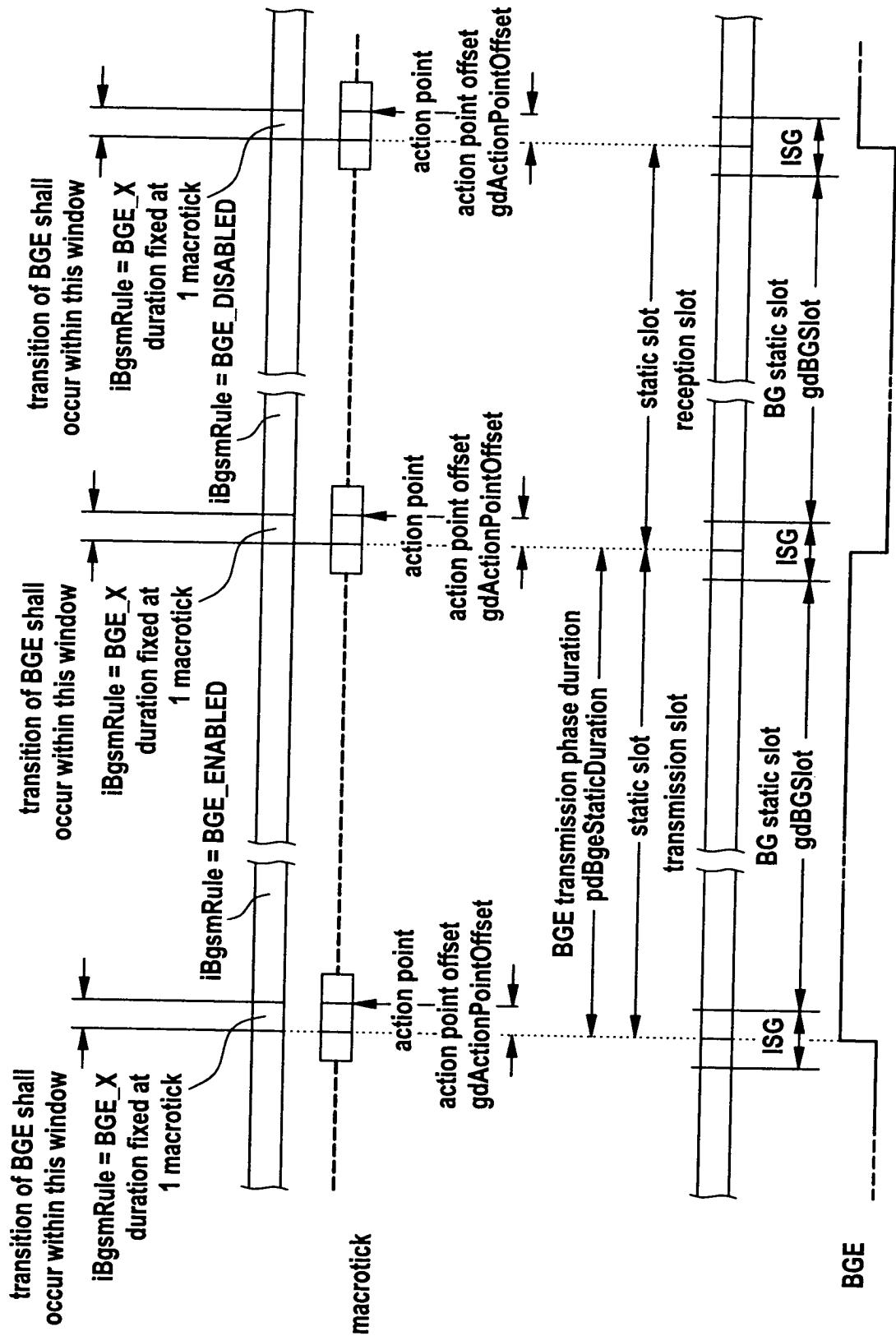


Fig. 92 transition of BGE shall occur within this window

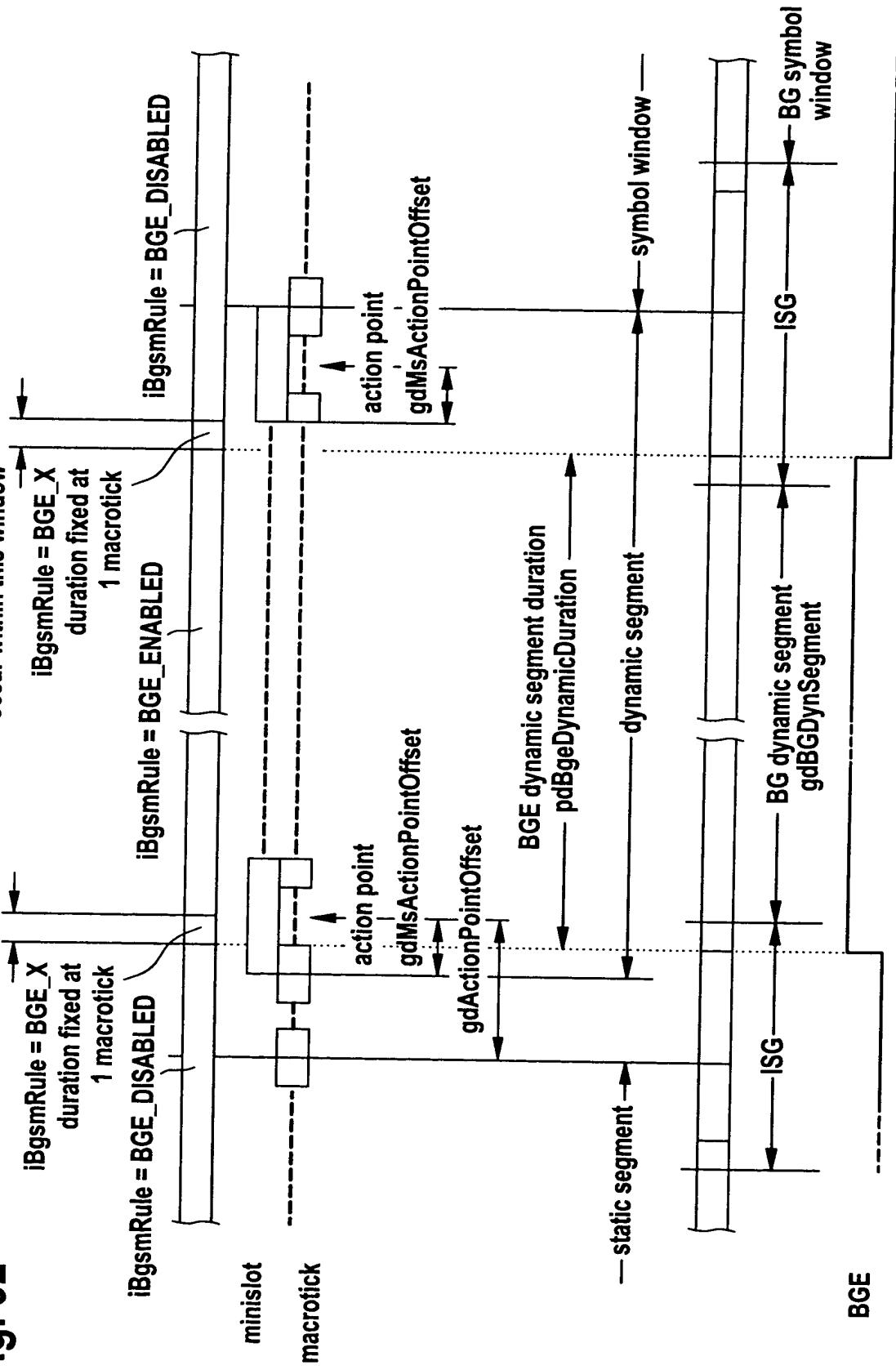


Fig. 93

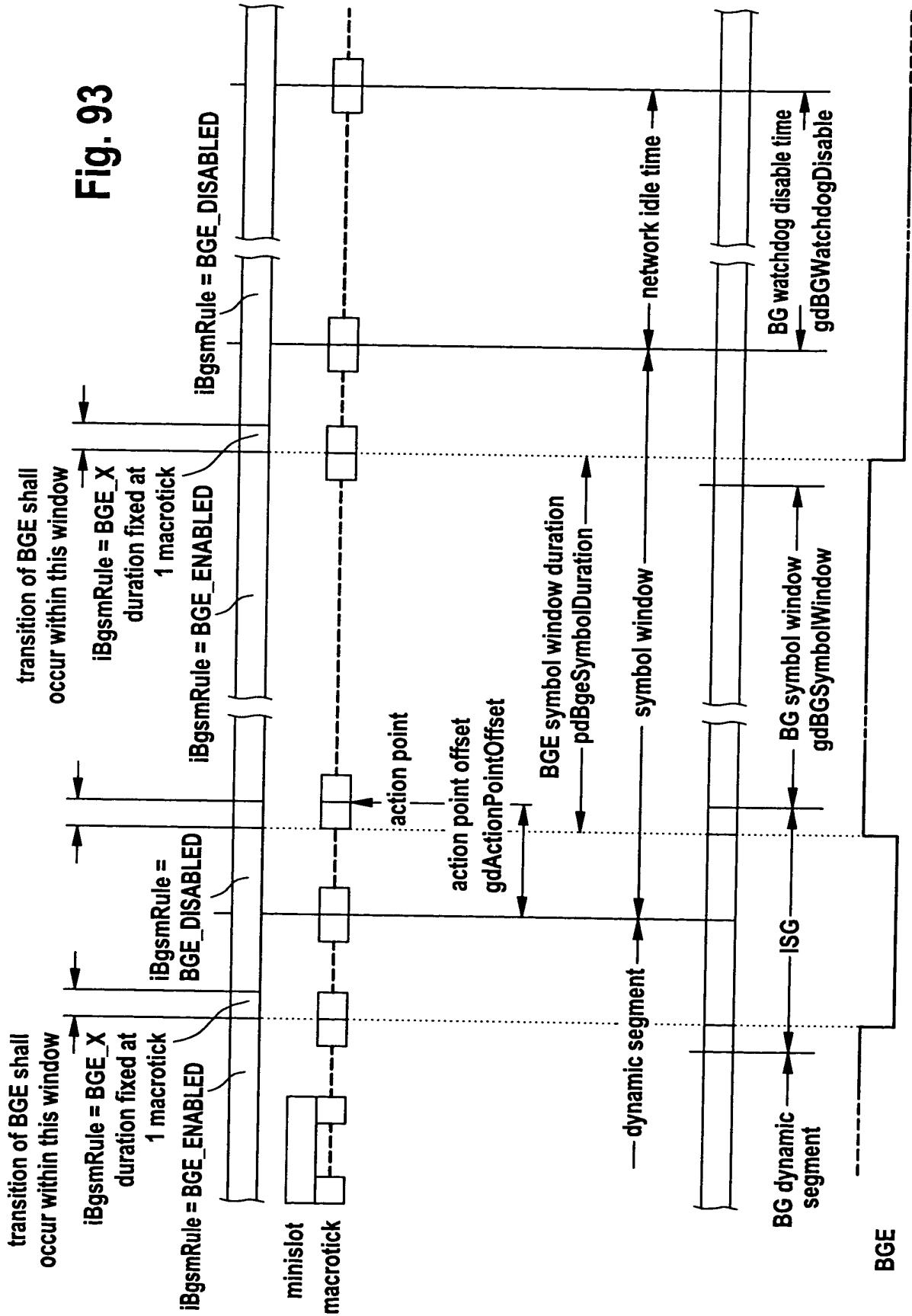


Fig. 94

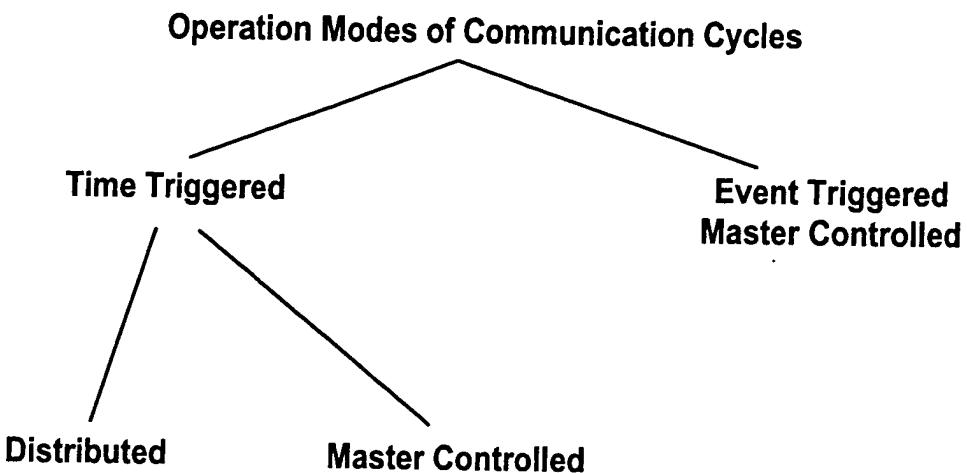


Fig. 95

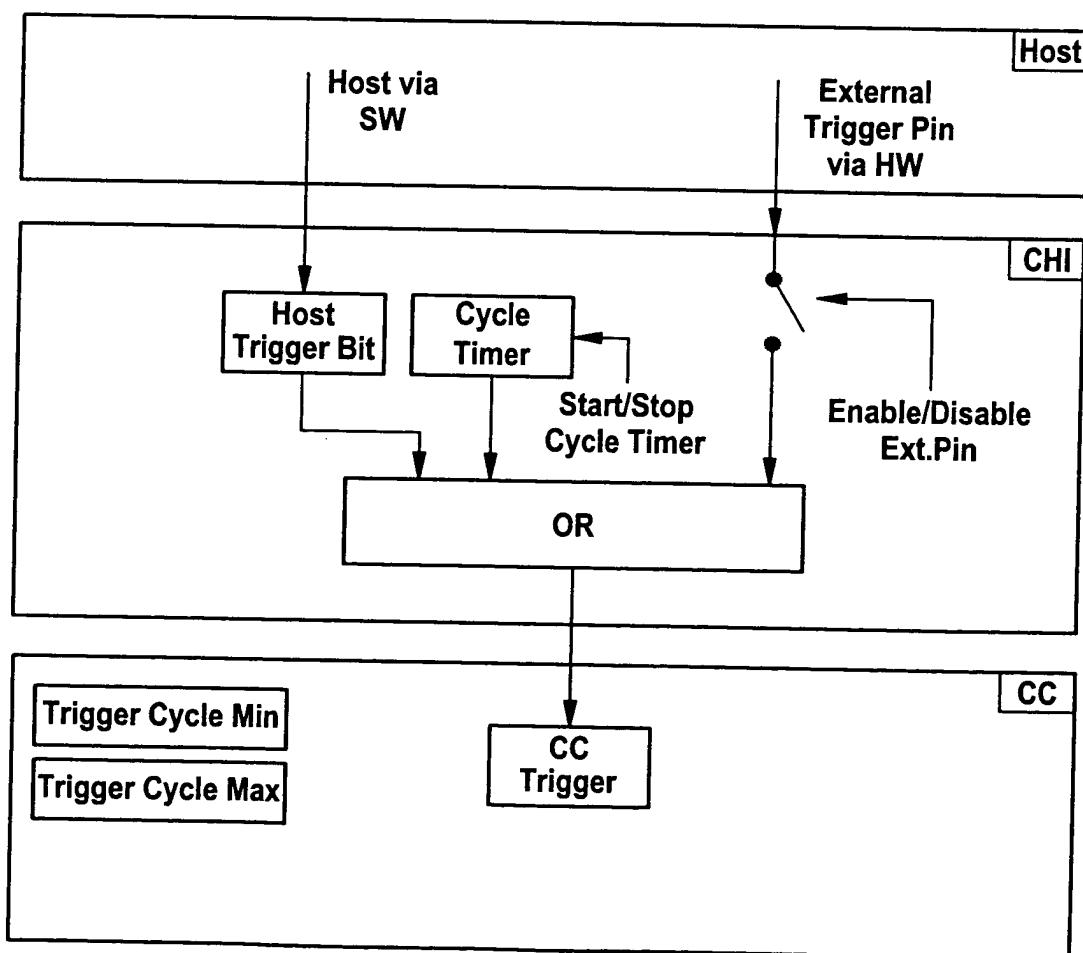
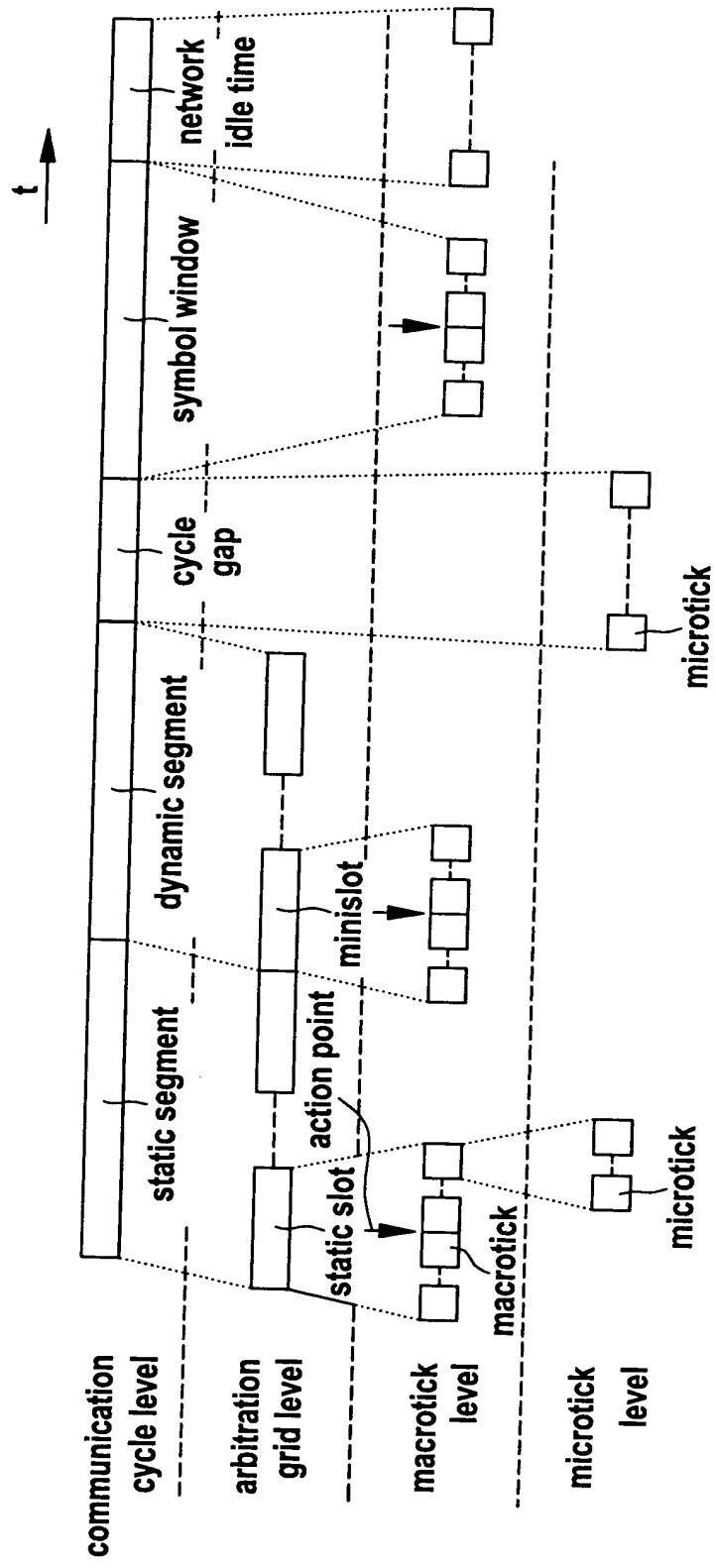


Fig. 96



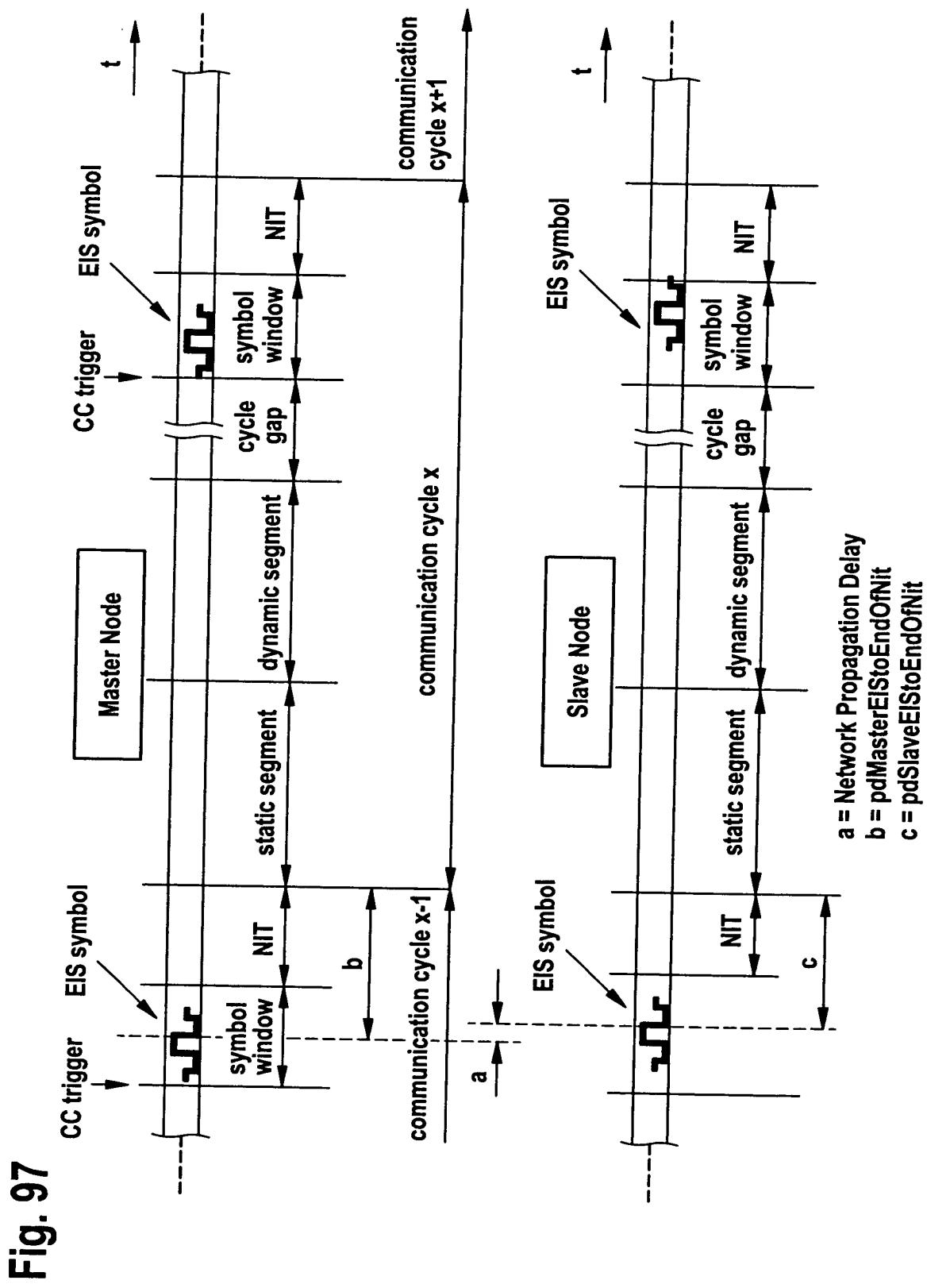


Fig. 97

Fig. 98

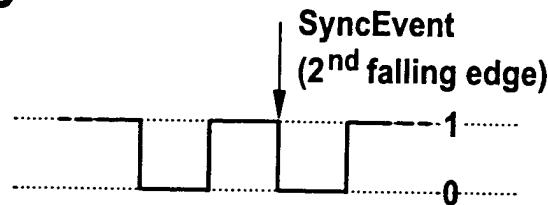


Fig. 99

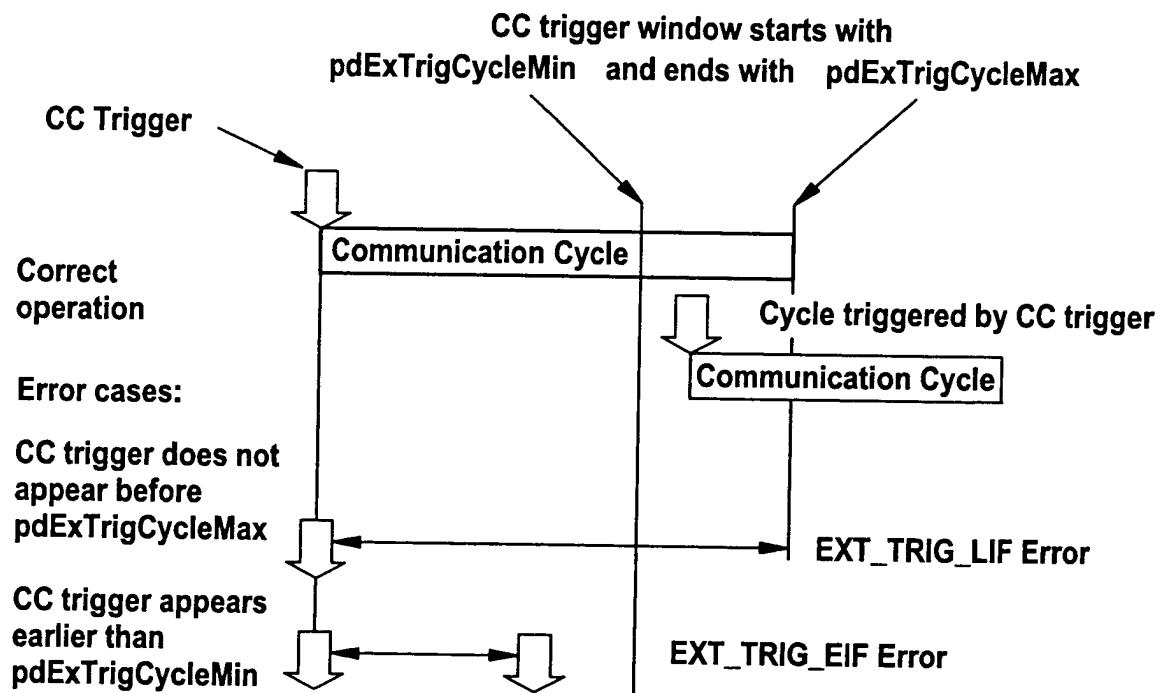


Fig. 100

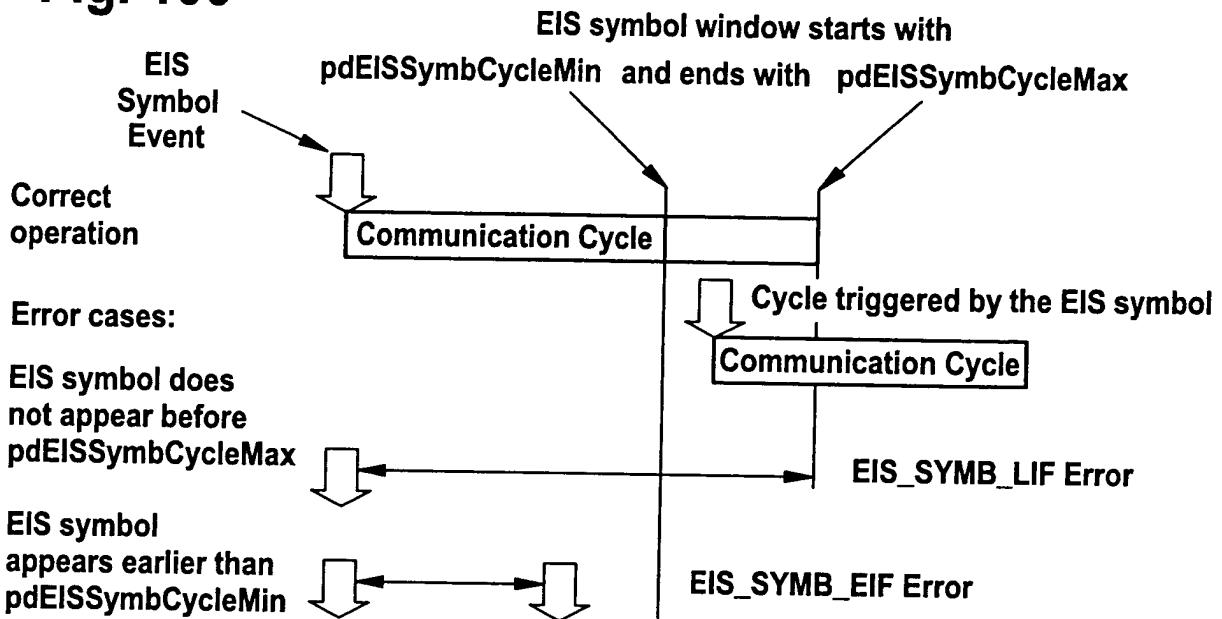


Fig. 101

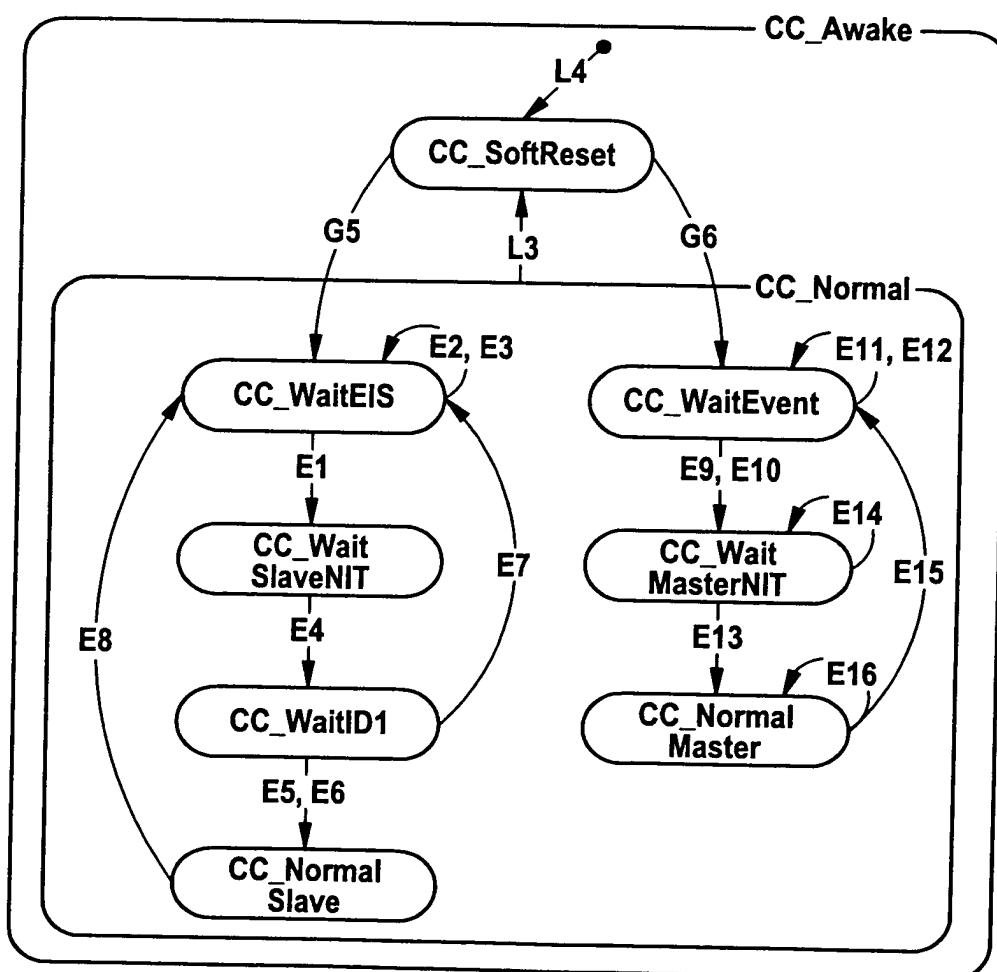


Fig. 102

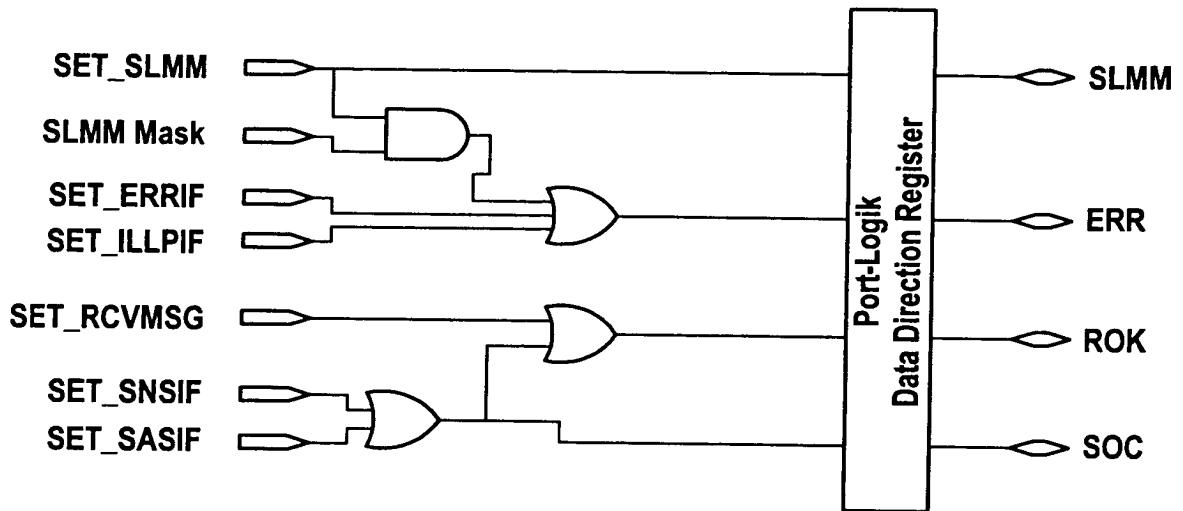


Fig. 103

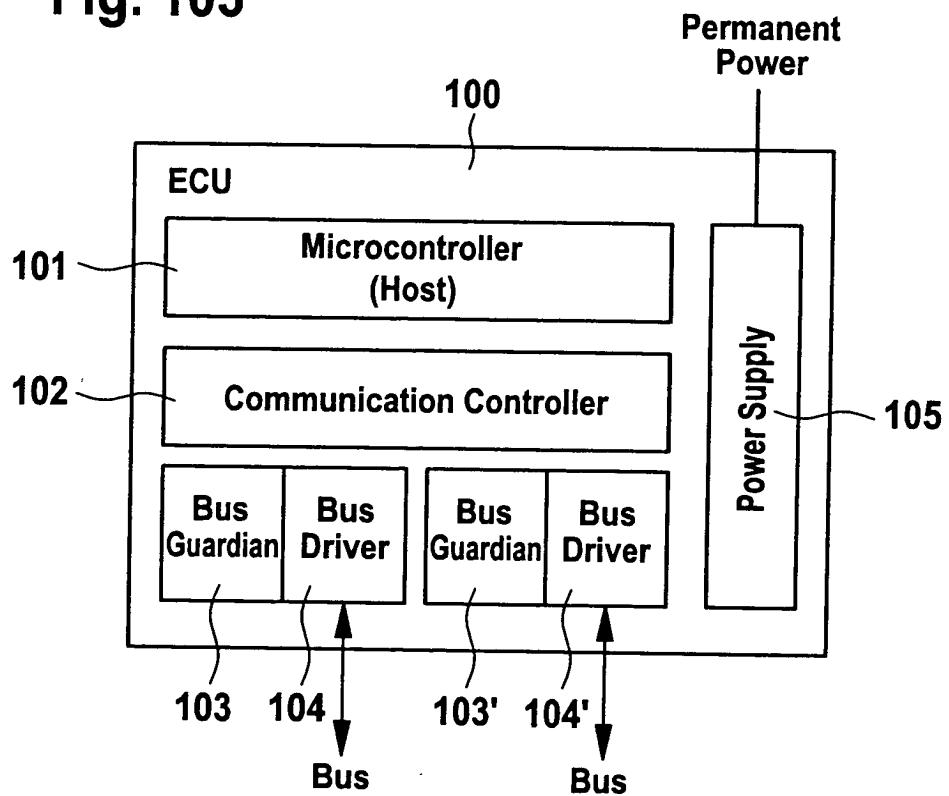


Fig. 104

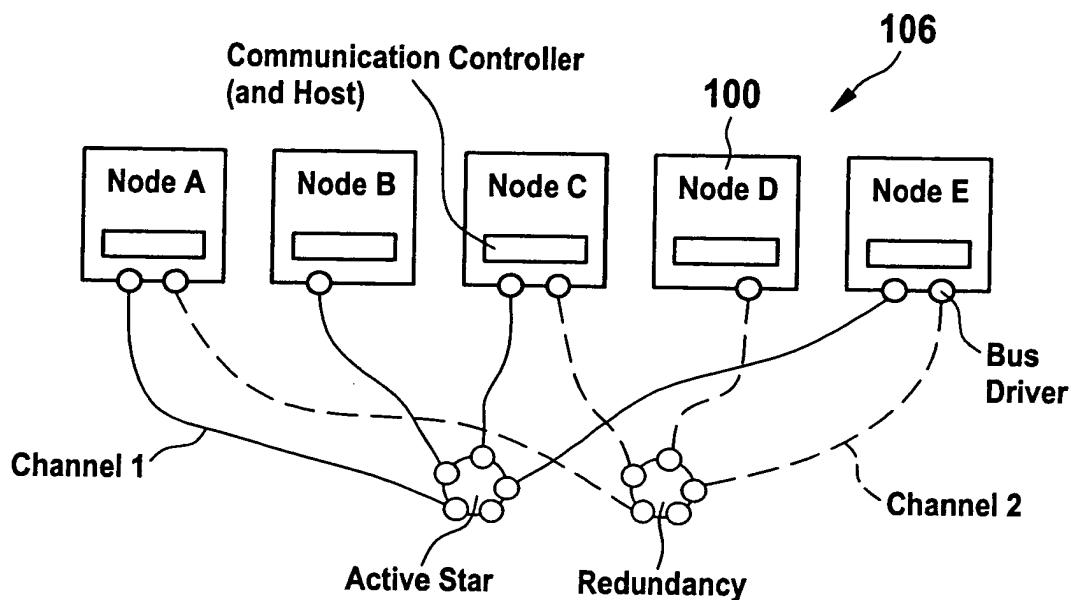


Fig. 105

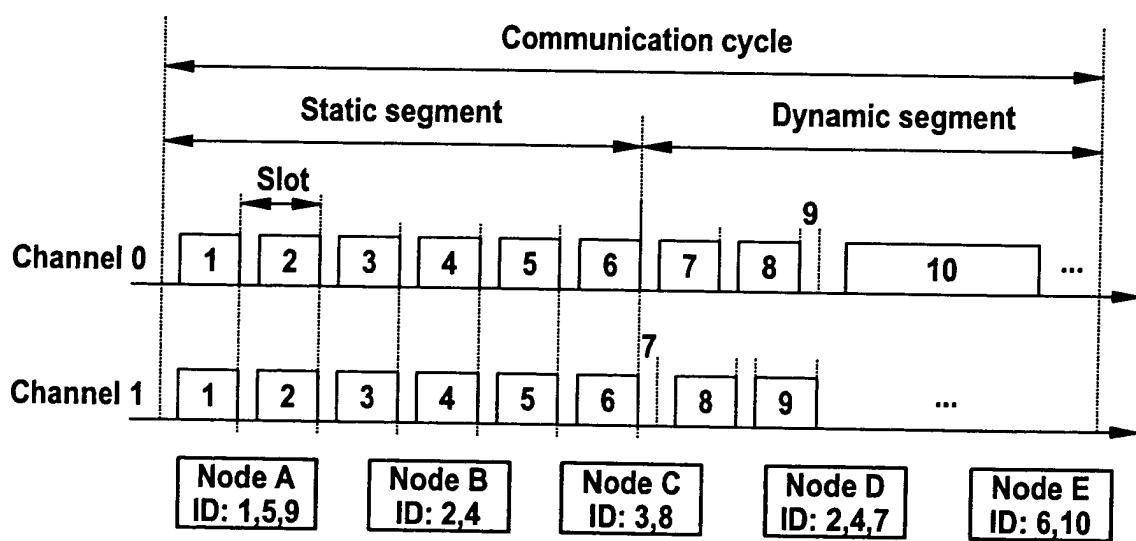


Fig. 106

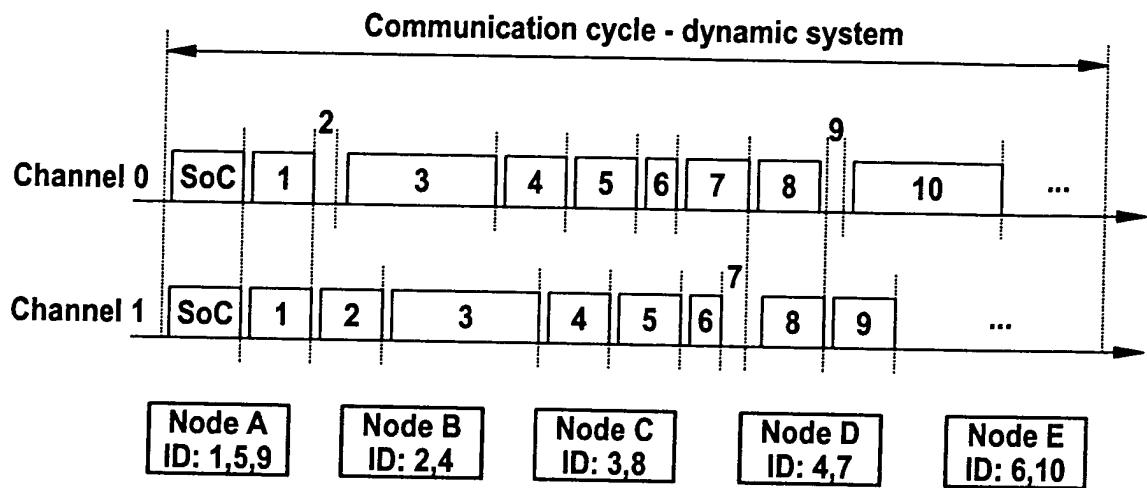


Fig. 107

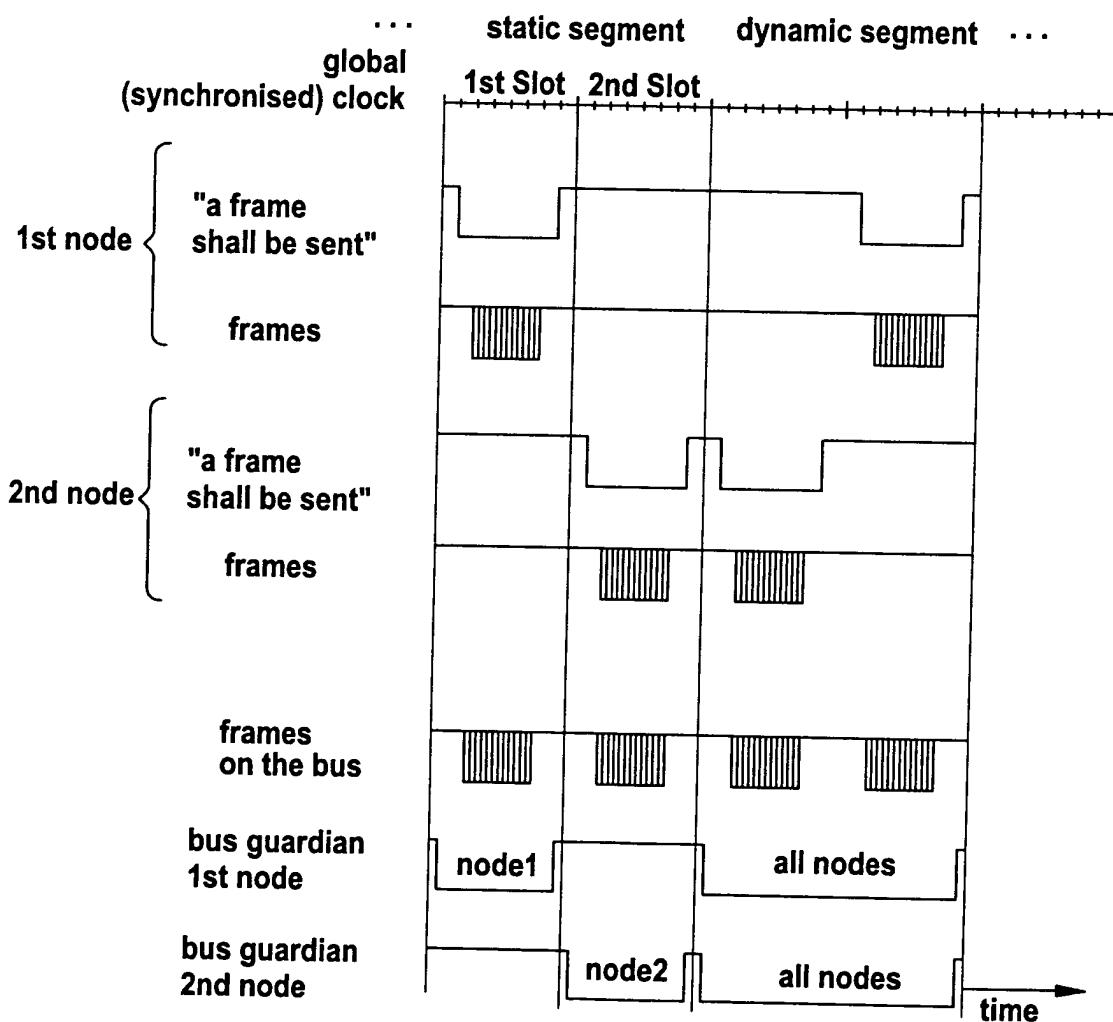


Fig. 108

Header 5 Bytes										Data 0 ... 246 Bytes		CRC Code 3 Bytes	
Res	Frame ID	Sync	DLC	H-CRC	NF	CYCO	Message ID			Data		CRC	

4 12 1 7 9 1 6 16 0...1968 24

Fig. 109

Header 2 Bytes			Data 0 ... 12 Bytes			CRC Code (15 Bit) + Frame Completion Bit		
ID	RES	LEN		DATA		CRC	FCB	

8 4 4 0 ... 96 15 1

Fig. 110

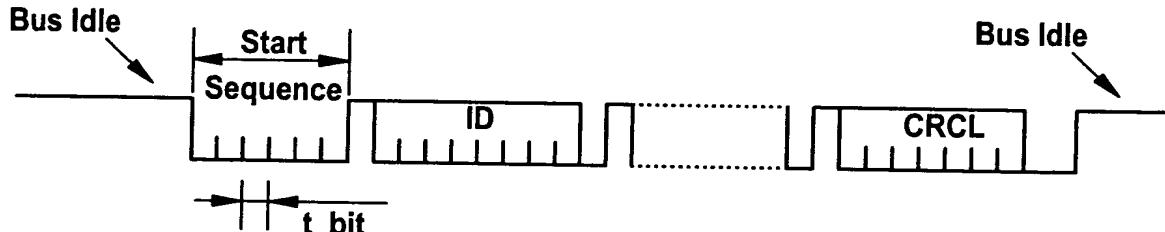


Fig. 111

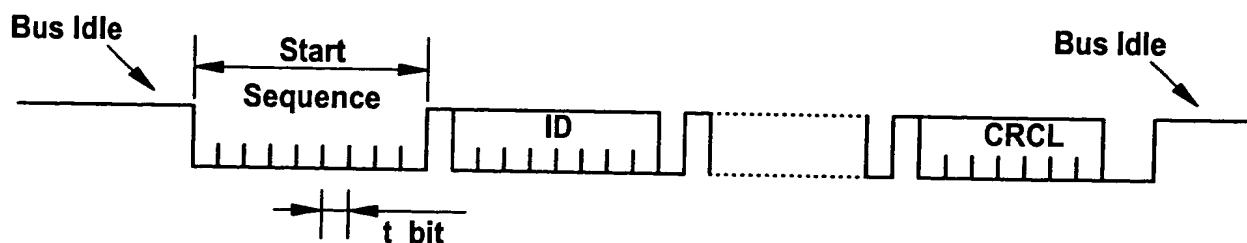


Fig. 112

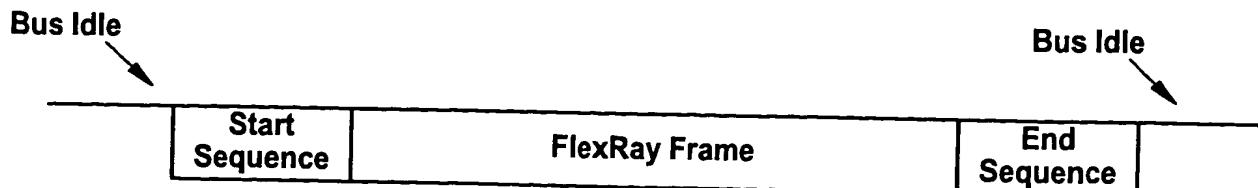


Fig. 113

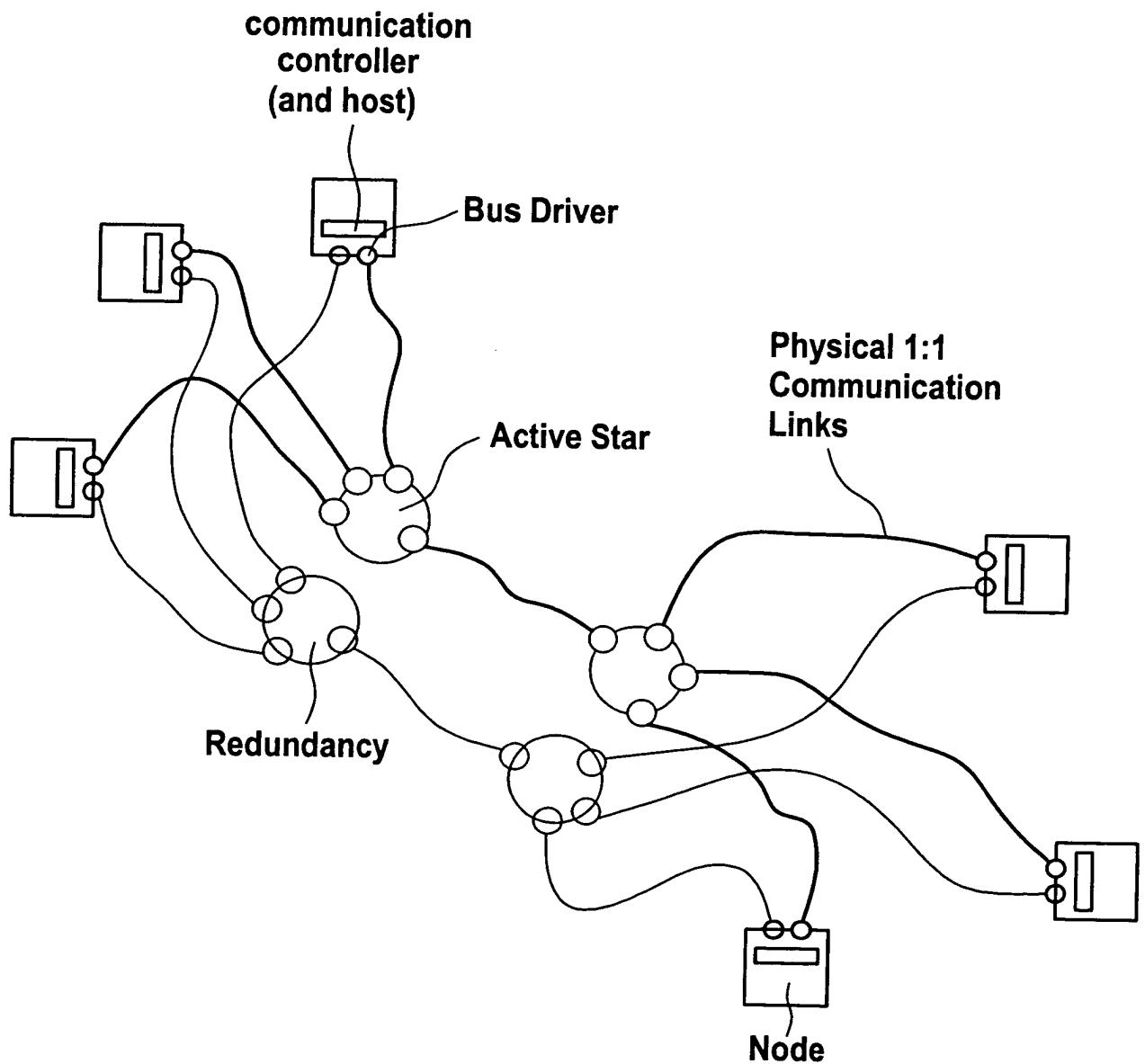


Fig. 114

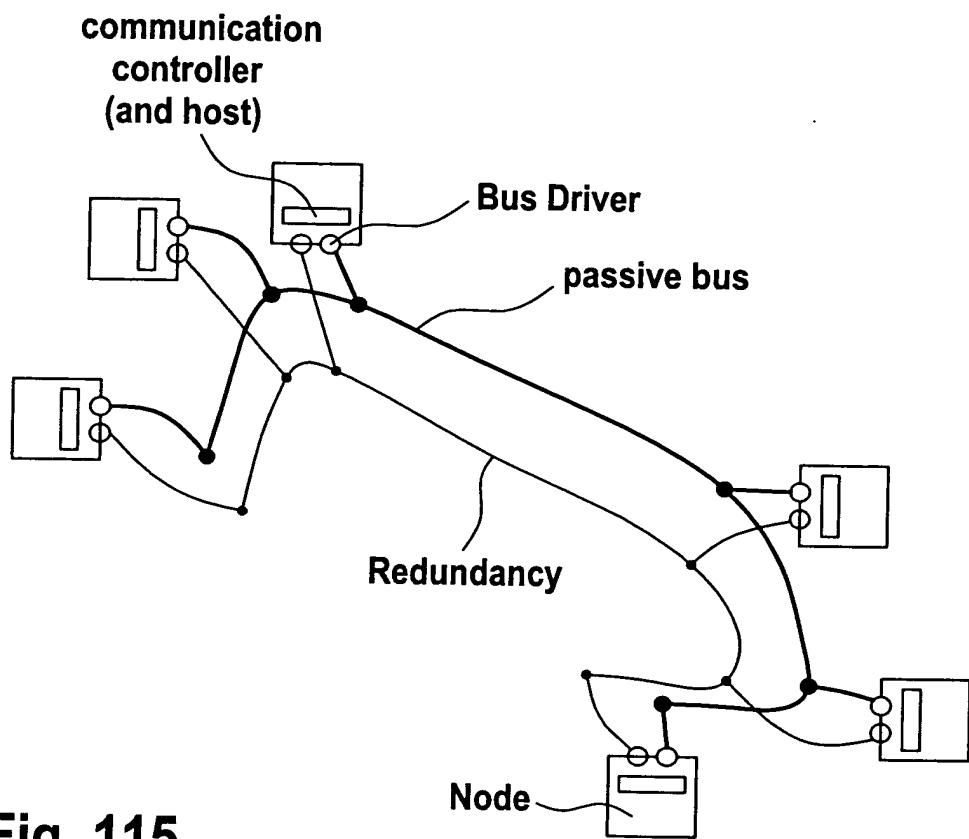


Fig. 115

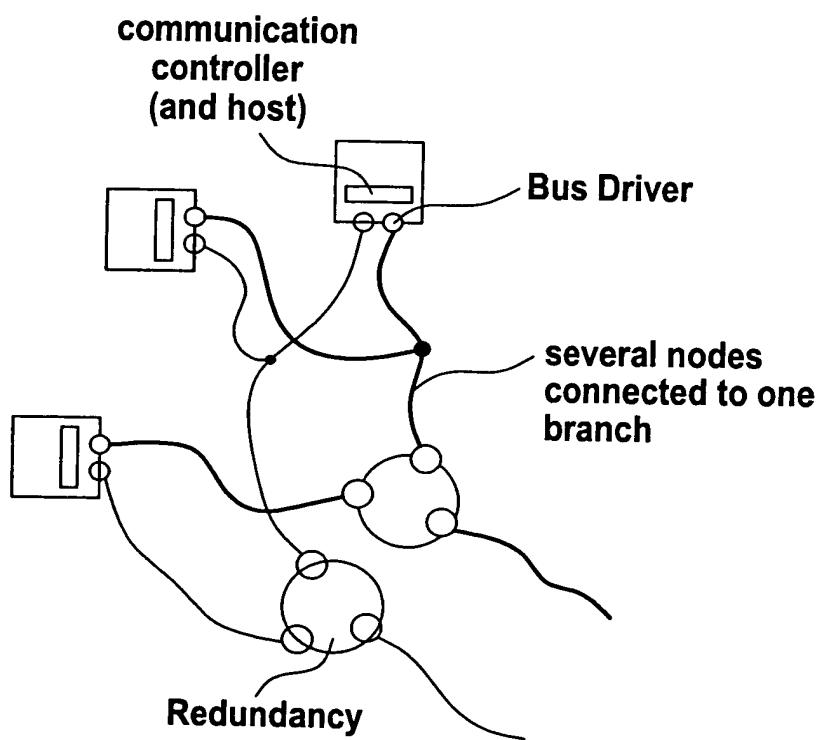


Fig. 116

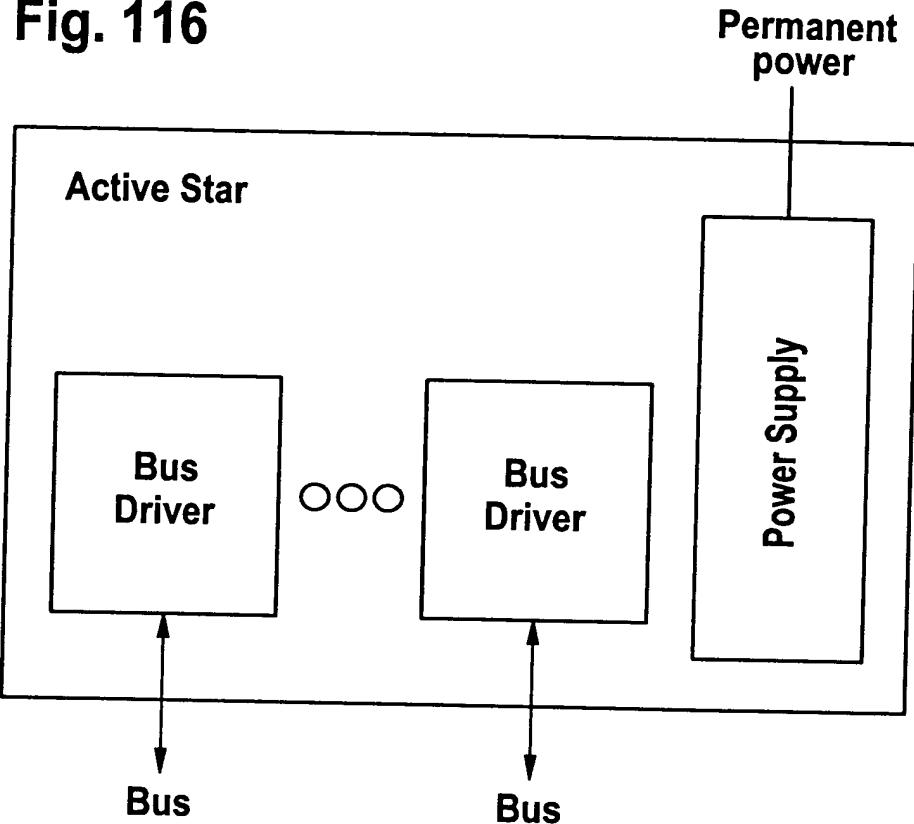


Fig. 117

